

具有±70V 总线故障保护、信号增强功能(SIC) 和待机模式的 CAN FD 收发器

UMCAN1472VS8 SOP8
UMCAN1472NS8 SOP8
UMCAN1472VDA DFN8 3.0×3.0
UMCAN1472NDA DFN8 3.0×3.0

1 描述

UMCAN1472 是高速 CAN 收发器，可在控制器局域网 (CAN) 协议控制器和物理双线式 CAN 总线之间提供接口。该收发器专用于汽车业的高速 CAN 应用，可以为(微控制器中的) CAN 协议控制器提供发送和接收差分信号的功能。

UMCAN1472改进了电磁兼容性 (EMC)和静电放电 (ESD)性能，并具有以下特点：

- ±70V 总线故障保护
- 电源关闭时，CAN总线具有良好的无源性能
- 具有总线唤醒功能的超低电流待机模式
- 即使不使用共模扼流圈，也具有出色的电磁兼容 (EMC) 性能
- 带有V_{IO}管脚的型号可直接连接电源电压为3.3V和5V的微控制器

UMCAN1472实现了ISO 11898-2:2024和SAE J2284-1至SAE J2284-5中定义的CAN物理层，并与高速经典CAN和CAN FD收发器完全兼容。UMCAN1472具备符合 ISO 11898-2:2024 参数集C的定义的信号改善功能(SIC)。CAN信号改善功能可显著减少网络中的信号振铃现象，从而使CAN FD通信能够在更大规模的拓扑结构中可靠运行。此外，UMCAN1472 还具备更严格的位时序对称性性能，可支持最高8 Mbit/s的CAN FD通信。这些特性使 UMCAN1472 成为所有类型HS-CAN网络的理想选择，特别适用于需要通过总线实现唤醒功能的待机模式节点。

2 应用

- 汽车工业中的高速 CAN 应用
- 基础设施和农业设备
- 电梯
- 联网的传感器/执行器

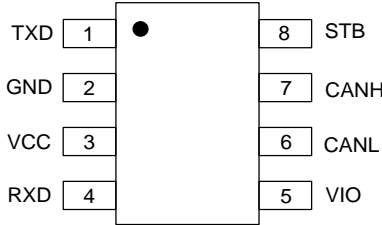
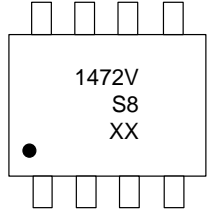
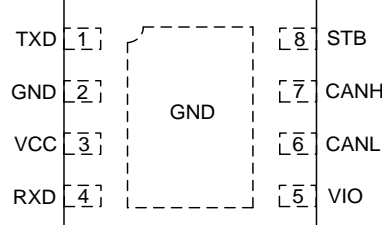
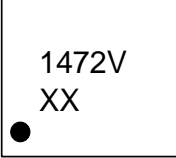
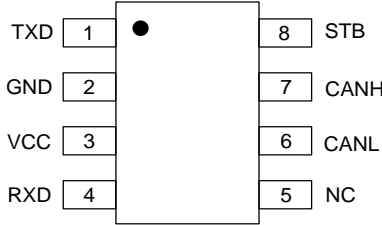
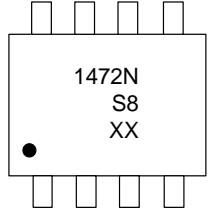
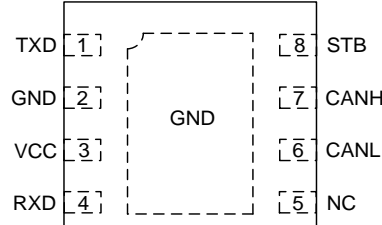
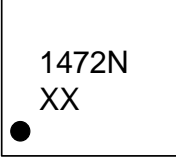
3 特性

- 完全符合ISO 11898-2:2024、SAE J2284-1至SAE J2284-5和SAE J1939-14标准
- 保护特性：
 - 总线故障保护：±70V
 - ±8kV IEC 61000-4-2 接触放电
- 超低电流待机模式，具有本地和总线唤醒功能
- 具备信号改善功能 (SIC)
- 低电磁辐射(EME)和高电磁抗扰度(EMI)，符合拟议的EMC标准IEC 62228-3和SAE J2962-2标准
- 数据传输速率高达 8Mbps

4 Ordering Information

| Part Number | Marking Code | Package Type | Shipping Qty |
|--------------|--------------|--------------|----------------------------|
| UMCAN1472VS8 | 1472VS8 | SOP8 | 3000pcs/13Inch Tape & Reel |
| UMCAN1472VDA | 1472V | DFN8 3.0×3.0 | 3000pcs/13Inch Tape & Reel |
| UMCAN1472NS8 | 1472NS8 | SOP8 | 3000pcs/13Inch Tape & Reel |
| UMCAN1472NDA | 1472N | DFN8 3.0×3.0 | 3000pcs/13Inch Tape & Reel |

5 Pin Configuration and Function

| | |
|---|--|
|  |  <p>XX: Week Code UMCAN1472VS8 SOP8</p> |
|  |  <p>XX: Week Code UMCAN1472VDA DFN8 3.0×3.0</p> |
|  |  <p>XX: Week Code UMCAN1472NS8 SOP8</p> |
|  |  <p>XX: Week Code UMCAN1472NDA DFN8 3.0×3.0</p> |

5 Pin Configuration and Function (continued)

Table 5-1. Pin Functions

| Pin No. | Symbol | Description |
|---------|-----------------|---|
| 1 | TXD | Transmit data input |
| 2 | GND | Ground (Note 1) |
| 3 | V _{CC} | Supply voltage |
| 4 | RXD | Receive data output; reads out data from the bus lines |
| 5 | NC | Not connected in UMCAN1472NS8 and UMCAN1472NDA version |
| | V _{IO} | Supply voltage for I/O level adapter in UMCAN1472VS8 and UMCAN1472VDA version |
| 6 | CANL | Low-level CAN bus line |
| 7 | CANH | High-level CAN bus line |
| 8 | STB | Standby mode control input |

Note 1: DFN8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

6 Specifications

6.1 Recommended Operating Conditions

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------|----------------------------------|------------|-----|-----|-----|------|
| V _{CC} | Bus supply voltage | | 4.5 | | 5.5 | V |
| V _{IO} | Supply voltage I/O level shifter | | 2.9 | | 5.5 | V |
| T _A | Operating ambient temperature | | -40 | | 125 | °C |

6.2 Absolute Maximum Ratings (Note 1, 2, 3)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|------------------|--|------------|------|-----|----------------------|------|
| V _{CC} | Bus supply voltage | | -0.3 | | +7 | V |
| V _{IO} | Supply voltage I/O level shifter | | -0.3 | | +7 | V |
| V _{BUS} | Voltage range on CANH, CANL | | -70 | | +70 | V |
| V _{DIF} | Voltage range between CANH and CANL | | -40 | | +40 | V |
| V _I | Voltage range on STB | Note 4 | -0.3 | | V _{IO} +0.3 | V |
| | Voltage range on TXD | Note 4 | -0.3 | | V _{IO} +0.3 | V |
| V _O | Voltage range on RXD | Note 4 | -0.3 | | V _{IO} +0.3 | V |
| V _{trt} | Transient voltage on CANH, CANL pins (Note 5) | pulse 1 | -100 | | | V |
| | | pulse 2a | | | +75 | V |
| | | pulse 3a | -150 | | | V |
| | | pulse 3b | | | +100 | V |
| V _{ESD} | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 | All pins | | ±8 | | kV |
| | Contact discharge, per IEC 61000-4-2 | Bus pins | | ±8 | | kV |
| I _{LU} | Latch up, per JEDEC JESD78 | Class II | | 200 | | mA |
| T _{VJ} | Virtual junction temperature | | -40 | | 150 | °C |
| T _{STG} | Storage temperature | | -55 | | 150 | °C |

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

Note 2: All voltage values, except differential I/O bus voltages, are with respect to ground terminal.

Note 3: V_{IO} = V_{CC} in non-VIO product variants.

Note 4: Maximum voltage should never exceed 7 V.

Note 5: Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

6.3 Electrical Characteristics (Static) (Note 1)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|--|--|---|-------------|-----|-------------|---------------|
| Supply; pin VCC | | | | | | |
| $V_{UVD(STB)}$ | Standby undervoltage detection voltage on pin VCC | | 3 | 3.6 | 4.5 | V |
| $V_{UVD(SWOFF)VCC}$ | Switch-off undervoltage detection voltage on pin VCC | Variants without VIO | 1.2 | 1.5 | 2.5 | V |
| I_{CC} | Supply current | Variants without a VIO pin; STB = V_{CC} ; TXD = V_{CC} | | 10 | 17.5 | μA |
| | | Variants with a VIO pin; STB = V_{IO} ; TXD = V_{IO} | | 0.4 | 1 | μA |
| | | STB = 0 V; TXD = V_{IO} | | 4 | 10 | mA |
| | | STB = 0 V; TXD = 0 V | 20 | 40 | 60 | mA |
| | | STB = 0 V; TXD = 0 V; short circuit on bus lines; $-3\text{V} < (\text{CANH}=\text{CANL}) < 18\text{V}$ | | 73 | 110 | mA |
| I/O level adapter supply; pin VIO | | | | | | |
| $V_{UVD(SWOFF)VIO}$ | Switch-off undervoltage detection voltage on pin VIO | Variants with a VIO pin | 1.2 | 1.5 | 2.5 | V |
| I_{IO} | Supply current on pin VIO | STB = V_{IO} ; TXD = V_{IO} | | 8.5 | 20 | μA |
| | | STB = 0 V; TXD = V_{IO} | 5 | 10 | 35 | μA |
| | | STB = 0 V; TXD = 0 V | | 70 | 300 | μA |
| Standby mode control input; pin STB | | | | | | |
| V_{IH} | High-level input voltage | | $0.7V_{IO}$ | | | V |
| V_{IL} | Low-level input voltage | | | | $0.3V_{IO}$ | V |
| I_{IH} | High-level input current | STB = V_{IO} | -1 | | 1 | μA |
| I_{IL} | Low-level input current | STB = 0 V | -15 | | -1 | μA |

6.3 Electrical Characteristics (Static)---continued (Note 1)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--------------------------------------|---|-------------|-----|-------------|---------------|
| CAN transmit data input; pin TXD | | | | | | |
| V_{IH} | High-level input voltage | | $0.7V_{IO}$ | | | V |
| V_{IL} | Low-level input voltage | | | | $0.3V_{IO}$ | V |
| I_{IH} | High-level input current | $\text{TXD} = V_{IO}$ | -5 | | 5 | μA |
| I_{IL} | Low-level input current | $\text{TXD} = 0\text{V}$ | -270 | -60 | -30 | μA |
| C_I | Input capacitance | | | 5 | 10 | pF |
| CAN receive data output; pin RXD | | | | | | |
| I_{OH} | High-level output current | $\text{RXD} = V_{IO} - 0.4\text{V}$ | -9 | -3 | -1 | mA |
| I_{OL} | Low-level output current | $\text{RXD} = 0.4\text{V}$ | 1 | 3 | 12 | mA |
| Driver | | | | | | |
| $V_{O(\text{DOM})}$ | Dominant output voltage | $\text{STB} = 0\text{V}$; $\text{TXD} = 0\text{V}$; $t < t_{\text{TO}(\text{DOM})\text{TXD}}$; $V_{CC} = 4.75\text{V}$ to 5.25V | | | | |
| | | $50\Omega \leq R_L \leq 65\Omega$; pin CANH | 2.75 | 3.5 | 4.5 | V |
| | | $50\Omega \leq R_L \leq 65\Omega$; pin CANL | 0.5 | 1.5 | 2.25 | V |
| $V_{OD(\text{DOM})}$ | Dominant differential output voltage | $\text{STB} = 0\text{V}$; $\text{TXD} = 0\text{V}$; $t < t_{\text{TO}(\text{DOM})\text{TXD}}$; $V_{CC} = 4.75\text{V}$ to 5.25V | | | | |
| | | $50\Omega \leq R_L \leq 65\Omega$ | 1.5 | | 3 | V |
| | | $45\Omega \leq R_L \leq 70\Omega$ | 1.4 | | 3.3 | V |
| | | $R_L = 2240\Omega$ | 1.5 | | 5 | V |

6.3 Electrical Characteristics (Static)---continued (Note 1)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-----------------------|---|--|-------------|-------------|-------------|------|
| $V_{\text{SYM(DOM)}}$ | Dominant output voltage symmetry, $V_{CC} - \text{CANH} - \text{CANL}$ | $\text{STB} = 0\text{V}$; $\text{TXD} = 0\text{V}$; $t < t_{\text{TO(DOM)TXD}}$; $R_L = 60\Omega$ | -400 | | 400 | mV |
| $V_{\text{CM(STEP)}}$ | Common mode voltage step | see Figure 7-4 | -150 | | 150 | mV |
| $V_{\text{CM(PP)}}$ | Peak-to-peak common mode voltage | See figure 7-4 | -300 | | 300 | mV |
| $V_{\text{O(REC)}}$ | Recessive output voltage | $\text{STB} = 0\text{V}$; $\text{TXD} = V_{\text{IO}}$; $R_L = \text{open}$ | 2 | $0.5V_{CC}$ | 3 | V |
| | | $\text{STB} = 0\text{V}$; $\text{TXD} = V_{\text{IO}}$; $R_L = 60\Omega$ | 2.137 | | 2.887 | V |
| $V_{\text{OD(REC)}}$ | Recessive differential output voltage | $\text{STB} = 0\text{V}$; $\text{TXD} = V_{\text{IO}}$; $R_L = \text{open}$ | -50 | | 50 | mV |
| $V_{\text{O(STB)}}$ | Bus output voltage, Standby Mode | $\text{STB} = V_{\text{IO}}$; $\text{TXD} = V_{\text{IO}}$; $R_L = \text{open}$ | -100 | | 100 | mV |
| $V_{\text{OD(STB)}}$ | Bus differential output voltage, Standby Mode | $\text{STB} = V_{\text{IO}}$; $\text{TXD} = V_{\text{IO}}$; $R_L = \text{open}$ | -200 | | 200 | mV |
| $V_{\text{SYM(TX)}}$ | Transmitter output voltage symmetry, $(\text{CANH} + \text{CANL})/V_{CC}$ | $\text{STB} = 0\text{V}$; $\text{TXD} = 250\text{kHz}$, 1MHz , 2.5MHz ; $R_L = 60\Omega$; $C_{\text{SPLIT}} = 4.7\text{nF}$; see Figure 7-2 | $0.9V_{CC}$ | | $1.1V_{CC}$ | V |
| $I_{\text{OS(DOM)}}$ | Dominant short-circuit output current | $\text{STB} = 0\text{V}$; $\text{TXD} = 0\text{V}$; $V_{CC} = 5\text{V}$; $\text{CANH} = -15\text{V}$ to 40V ; $\text{CANL} = \text{open}$ | -100 | -70 | | mA |
| | | $\text{STB} = 0\text{V}$; $\text{TXD} = 0\text{V}$; $V_{CC} = 5\text{V}$; $\text{CANL} = -15\text{V}$ to 40V ; $\text{CANH} = \text{open}$ | | 70 | 100 | mA |
| $I_{\text{OS(REC)}}$ | Recessive short-circuit output current | $\text{STB} = 0\text{V}$; $\text{TXD} = V_{\text{IO}}$; $-27\text{V} \leq \text{CANH} = \text{CANL} \leq 32\text{V}$ | -5 | | 5 | mA |
| Receiver | | | | | | |
| V_{TH} | Differential receiver threshold voltage, Normal mode | $\text{STB} = 0\text{V}$; $-30\text{V} \leq \text{CANH}$, $\text{CANL} \leq 30\text{V}$ | 0.5 | | 0.9 | V |
| $V_{\text{ID(DOM)}}$ | Receiver dominant voltage, Normal mode | $\text{STB} = 0\text{V}$; $-30\text{V} \leq \text{CANH}$, $\text{CANL} \leq 30\text{V}$ | 0.9 | | 9 | V |
| $V_{\text{ID(REC)}}$ | Receiver recessive voltage, Normal mode | $\text{STB} = 0\text{V}$; $-30\text{V} \leq \text{CANH}$, $\text{CANL} \leq 30\text{V}$ | -4 | | 0.5 | V |
| V_{HYS} | Differential receiver hysteresis voltage, Normal mode | $\text{STB} = 0\text{V}$; $-30\text{V} \leq \text{CANH}$, $\text{CANL} \leq 30\text{V}$ | 50 | | 300 | mV |

6.3 Electrical Characteristics (Static)---continued (Note 1)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---------------------------|--|--|------|-----|------|--------------------|
| $V_{TH(STB)}$ | Differential receiver threshold voltage, Standby mode | $STB = V_{IO}$; $-30\text{V} \leq \text{CANH, CANL} \leq 30\text{V}$ | 0.4 | | 1.15 | V |
| $V_{ID(DOM)STB}$ | Receiver dominant voltage, Standby mode | $STB = V_{IO}$; $-30\text{V} \leq \text{CANH, CANL} \leq 30\text{V}$ | 1.15 | | 9 | V |
| $V_{ID(REC)STB}$ | Receiver recessive voltage, Standby mode | $STB = V_{IO}$; $-30\text{V} \leq \text{CANH, CANL} \leq 30\text{V}$ | -4 | | 0.4 | V |
| $I_{LKG(PD)}$ | Unpowered Leakage current | $V_{CC} = V_{IO} = 0\text{V}$ or shorted to GND via $47\text{k}\Omega$; $\text{CANH} = \text{CANL} = 5\text{V}$ | -5 | | 5 | μA |
| R_I | Input resistance | $STB = 0\text{V}$; $\text{TXD} = V_{IO}$; $-2\text{V} \leq \text{CANH, CANL} \leq 7\text{V}$ | 15 | 30 | 40 | $\text{k}\Omega$ |
| ΔR_I | Input resistance deviation, $[1 - (R_{IN(CANH)} / R_{IN(CANL)})] \times 100\%$ | $STB = 0\text{V}$; $\text{TXD} = V_{IO}$; $-2\text{V} \leq \text{CANH, CANL} \leq 7\text{V}$ | -3 | | 3 | % |
| R_{ID} | Differential input resistance | $STB = 0\text{V}$; $\text{TXD} = V_{IO}$; $-2\text{V} \leq \text{CANH, CANL} \leq 7\text{V}$ | 30 | 60 | 80 | $\text{k}\Omega$ |
| C_{IN} | Common-mode input capacitance to ground | | | | 20 | pF |
| C_{ID} | Differential input capacitance | | | | 10 | pF |
| $R_{I(ACTREC)}$ | Active recessive phase input resistance (Note2) | Bus dominant-to-recessive transition $2\text{V} \leq V_{CANH} \leq V_{CC}-2\text{V}$; $2\text{V} \leq V_{CANL} \leq V_{CC}-2\text{V}$; | 37.5 | | 62.5 | Ω |
| $R_{I(DIF)ACTREC}$ | Active recessive phase differential input resistance (Note 2) | $R_{I(DIF)ACTREC} = R_{I(ACTREC)CANH} + R_{I(ACTREC)CANL}$ (Note 3) | 75 | | 125 | Ω |
| Thermal Protection | | | | | | |
| $T_{J(SD)}$ | Thermal shutdown threshold | | | 185 | | $^{\circ}\text{C}$ |

Note 1: $V_{IO} = V_{CC}$ in non-VIO product variants.

Note 2: Active recessive phases are not DC states and are only valid for a limited time after a dominant-to-recessive transition on pin TXD. The maximum value specified is lower than proscribed in ISO11898-2:2024 parameter set C (a lower value is preferred).

Note 3: Both conditions and the maximum specified values are tighter, thus better than proscribed in ISO11898-2:2024 parameter set C.

6.4 Electrical Characteristics (Dynamic) (Note 7)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|--|---|-----|-----|-----|------|
| CAN timing characteristics according to ISO 11898-2:2024; see Figure 7-1 and Figure 7-3 | | | | | | |
| $t_{D(\text{TXDL-RXDL})}$ | Delay time from TXD LOW to RXD LOW | STB = 0 V | | | 255 | ns |
| $t_{D(\text{TXDH-RXDH})}$ | Delay time from TXD HIGH to RXD HIGH | STB = 0 V | | | 255 | ns |
| CAN timing characteristics according to ISO 11898-2:2024; $V_{CC} = 4.75\text{V}$ to 5.25V; see Figure 7-1, Figure 7-3 and Figure 7-5 | | | | | | |
| $t_{D(\text{TXD-BUSDOM})}$ | Delay time from TXD to bus dominant | STB = 0 V | | | 80 | ns |
| $t_{D(\text{TXD-BUSREC})}$ | Delay time from TXD to bus recessive | STB = 0 V | | | 80 | ns |
| $t_{D(\text{BUSDOM-RXD})}$ | Delay time from bus dominant to RXD | STB = 0 V | | | 110 | ns |
| $t_{D(\text{BUSREC-RXD})}$ | Delay time from bus recessive to RXD | STB = 0 V | | | 110 | ns |
| $t_{D(\text{TXDL-RXDL})}$ | Delay time from TXD LOW to RXD LOW | STB = 0 V | | | 190 | ns |
| $t_{D(\text{TXDH-RXDH})}$ | Delay time from TXD HIGH to RXD HIGH | STB = 0 V | | | 190 | ns |
| $t_{D(\text{TXD-BUSPASREC})\text{START}}$ | Delay time from TXD to bus passive recessive start | STB = 0 V | | | 530 | ns |
| $t_{D(\text{TXD-BUSACTREC})\text{START}}$ | Delay time from TXD to bus active recessive start | STB = 0 V | | | 120 | ns |
| $t_{D(\text{TXD-BUSACTREC})\text{END}}$ | Delay time from TXD to bus active recessive end | STB = 0 V | 355 | | | ns |
| CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C ($t_{\text{BIT}(\text{TXD})} \geq 125\text{ ns}$, up to 8 Mbit/s); $V_{CC} = 4.75\text{V}$ to 5.25V; see Figure 7-1 and Figure 7-3; (Note 2) | | | | | | |
| $\Delta t_{\text{BIT}(\text{BUS})}$ | Transmitted recessive bit width deviation | $\Delta t_{\text{BIT}(\text{BUS})} = t_{\text{BIT}(\text{BUS})} - t_{\text{BIT}(\text{TXD})}$ | -10 | | 10 | ns |
| Δt_{REC} | Receiver timing symmetry | $\Delta t_{\text{REC}} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{BUS})}$ | -20 | | 15 | ns |
| $\Delta t_{\text{BIT}(\text{RXD})}$ | Received recessive bit width deviation | $\Delta t_{\text{BIT}(\text{RXD})} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{TXD})}$ | -30 | | 20 | ns |

6.4 Electrical Characteristics (Dynamic) ---continued (Note 7)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|--|------|-----|-----|------|
| CAN FD timing characteristics according to ISO 11898-2:2016 and ISO 11898-2:2024; $V_{CC} = 4.75\text{V}$ to 5.25V; see Figure 7-1 and Figure 7-3 | | | | | | |
| $t_{\text{BIT}(\text{BUS})}$ | Transmitted recessive bit width | 2 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 500\text{ ns}$) | 490 | | 510 | ns |
| | | 5 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 200\text{ ns}$) | 190 | | 210 | ns |
| $t_{\text{BIT}(\text{RXD})}$ | Bit time on pin RXD (Note 1) | 2 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 500\text{ ns}$) | 470 | | 520 | ns |
| | | 5 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 200\text{ ns}$) | 170 | | 220 | ns |
| $\Delta t_{\text{BIT}(\text{BUS})}$ | Transmitted recessive bit width deviation | 2 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 500\text{ ns}$) $\Delta t_{\text{BIT}(\text{BUS})} = t_{\text{BIT}(\text{BUS})} - t_{\text{BIT}(\text{TXD})}$ | -65 | | 30 | ns |
| Δt_{REC} | Receiver timing symmetry | 2 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 500\text{ ns}$) $\Delta t_{\text{REC}} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{BUS})}$ | -65 | | 40 | ns |
| $\Delta t_{\text{BIT}(\text{RXD})}$ | Received recessive bit width deviation | 2 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 500\text{ ns}$) $\Delta t_{\text{BIT}(\text{RXD})} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{TXD})}$ | -100 | | 50 | ns |
| $\Delta t_{\text{BIT}(\text{BUS})}$ | Transmitted recessive bit width deviation | 5 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 200\text{ ns}$) | -45 | | 10 | ns |
| | | $\Delta t_{\text{BIT}(\text{BUS})} = t_{\text{BIT}(\text{BUS})} - t_{\text{BIT}(\text{TXD})}$ | | | | |
| Δt_{REC} | Receiver timing symmetry | 5 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 200\text{ ns}$) | -45 | | 15 | ns |
| | | $\Delta t_{\text{REC}} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{BUS})}$ | | | | |
| $\Delta t_{\text{BIT}(\text{RXD})}$ | Received recessive bit width deviation | 5 Mbit/s ($t_{\text{BIT}(\text{TXD})} = 200\text{ ns}$) $\Delta t_{\text{BIT}(\text{RXD})} = t_{\text{BIT}(\text{RXD})} - t_{\text{BIT}(\text{TXD})}$ | -80 | | 20 | ns |
| Dominant time-out time; pin TXD; (Note 3) | | | | | | |
| $t_{\text{TO}(\text{DOM})\text{TXD}}$ | TXD dominant time-out time | STB = 0 V; TXD = 0V | 0.8 | | 9 | ms |
| Bus wake-up times; pins CANH and CANL; see Figure 9-3; (Note 3, 4) | | | | | | |
| $t_{\text{WK}(\text{BUSDOM})}$ | Bus dominant wake-up time | STB = V_{IO} | 0.5 | | 1.8 | us |
| $t_{\text{WK}(\text{BUSREC})}$ | Bus recessive wake-up time | STB = V_{IO} | 0.5 | | 1.8 | us |
| $t_{\text{TO}(\text{WK})\text{BUS}}$ | Bus wake-up time-out time | STB = V_{IO} | 0.8 | | 9 | ms |
| $t_{\text{FLTR}(\text{WK})\text{BUS}}$ | Bus wake-up filter time | STB = V_{IO} | | | 1.8 | us |
| Mode transitions | | | | | | |
| $t_{\text{D}(\text{STB-NRM})}$ | Mode change time, from standby to normal | | | | 50 | us |
| $t_{\text{STARTUP}(\text{RXD})}$ | RXD start-up time | After wake-up detected (Note 5) | 4 | | 20 | us |

6.4 Electrical Characteristics (Dynamic) ---continued (Note 7)

$T_J = -40^{\circ}\text{C}$ to $+150^{\circ}\text{C}$; $V_{CC} = 4.5\text{V}$ to 5.5V ; $V_{IO} = 2.9\text{V}$ to 5.5V ; $R_L = 60\Omega$; $C_L = 100\text{pF}$ unless otherwise noted; Typical values are at $V_{CC} = 5\text{V}$, $V_{IO} = 3.3\text{V}$, $T_A = 25^{\circ}\text{C}$.

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------------------------------|----------------|------------|-----|-----|-----|------|
| IO filter; pin STB; (Note 6) | | | | | | |
| $t_{FLTR(IO)}$ | IO filter time | on pin STB | 5 | | 15 | us |

Note 1: Not tested in production; guaranteed by design.

Note 2: Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{BIT(TXD)} \geq 500\text{ ns}$, up to 2 Mbit/s) and B ($t_{BIT(TXD)} \geq 200\text{ ns}$, up to 5 Mbit/s).

Note 3: Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

Note 4: A dominant/recessive phase shorter than the min value is guaranteed not to be seen as a dominant/recessive bit; a dominant/recessive phase longer than the max value is guaranteed to be seen as a dominant/recessive bit.

Note 5: When a wake-up is detected, RXD start-up time is between the min and max values. RXD cannot be relied on below the min value; RXD can be relied on above the max value; see Figure 9-2.

Note 6: Pulses shorter than the min value are guaranteed to be filtered out; pulses longer than the max value are guaranteed to be processed.

Note 7: $V_{IO} = V_{CC}$ in non-VIO product variants.

7 Parameter Measurement Information

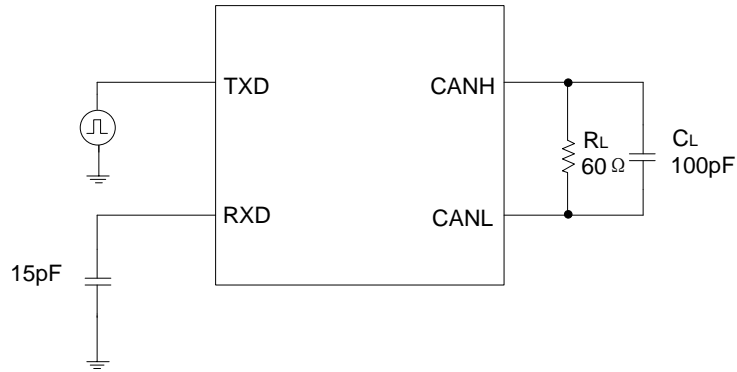


Figure 7-1. CAN transceiver timing test circuit

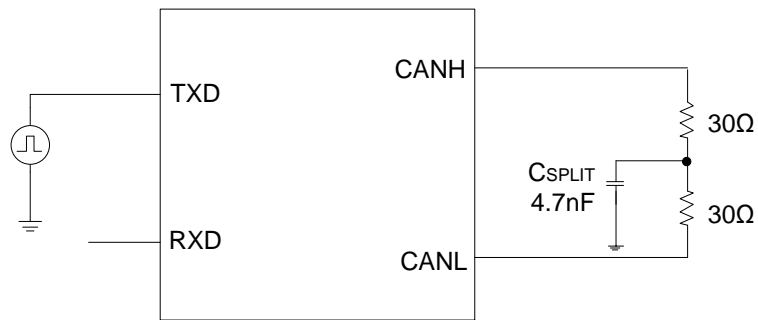


Figure 7-2. Test circuit for measuring transceiver transmitter driver symmetry

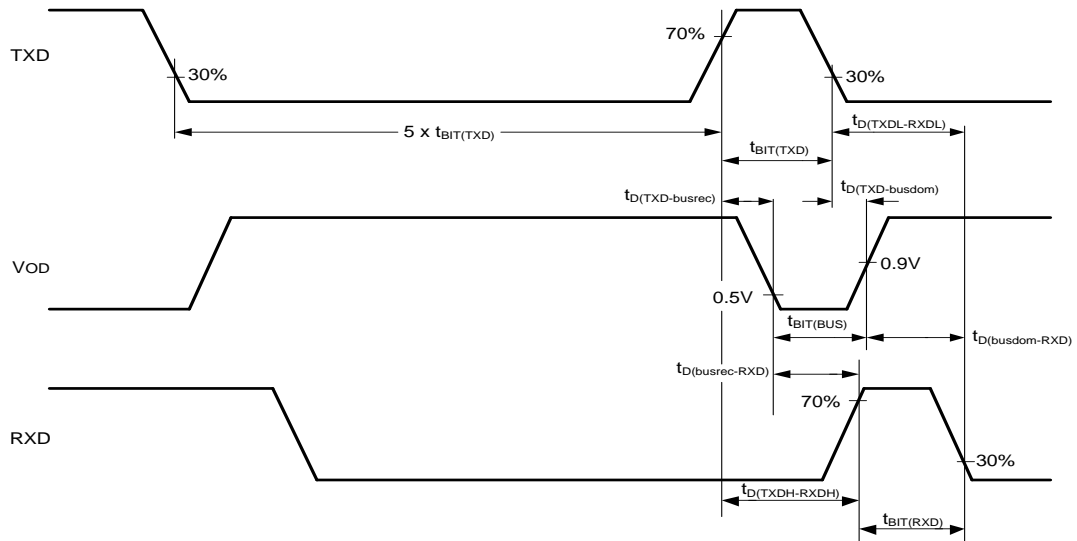


Figure 7-3. CAN transceiver timing diagram according to ISO 11898-2:2024

7 Parameter Measurement Information (continued)

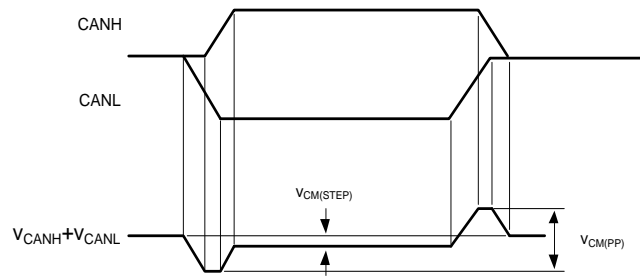
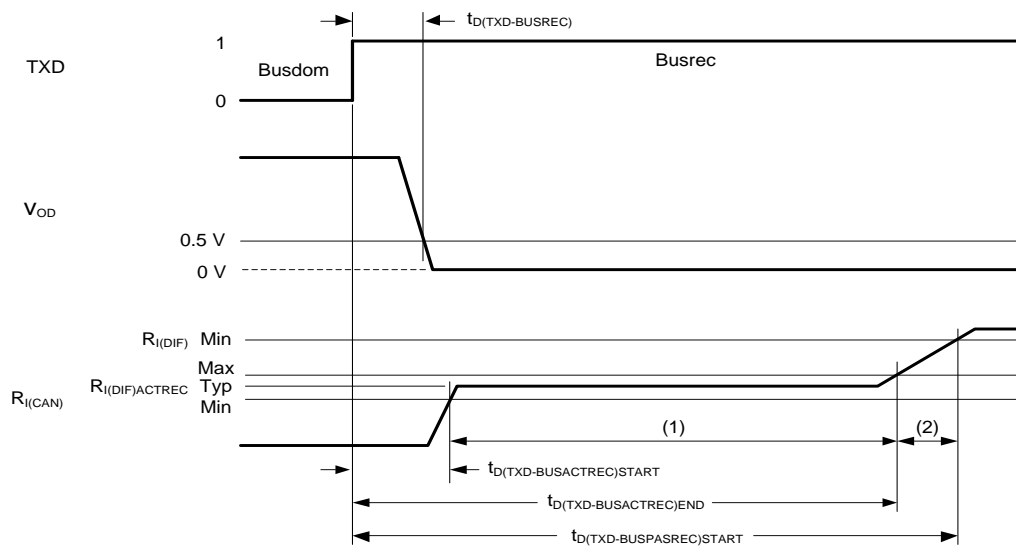


Figure 7-4. CAN bus common-mode voltage according to SAE 1939-14



Note 1 : (1) Active recessive phase (2) Release phase.

Figure 7-5. Transmitter impedance and timing diagram for dominant-to-passive recessive transition according to ISO11898-2:2024 parameter set C

8 Block diagram

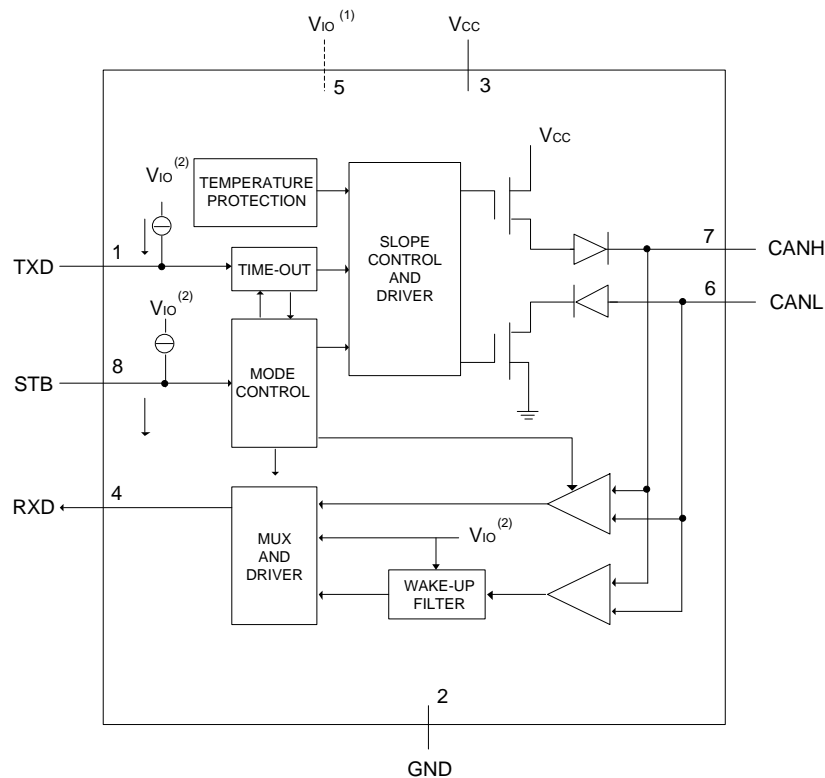


Figure 8-1. Block diagram

Note 1: Pin 5 is not connected in non-VIO product variants.

Note 2: $V_{IO} = V_{CC}$ in non-VIO product variants.

9 Detailed Description

9.1 Operating modes

The UMCAN1472 supports three operating modes, Normal, Standby and Off. The operating mode is selected via pin STB. See Table for a description of the operating modes under normal supply conditions.

| Mode | Inputs | | Outputs | |
|---------|---------|-----------|------------------|--|
| | Pin STB | Pin TXD | CAN driver | Pin RXD |
| Normal | LOW | LOW | dominant | LOW |
| | | HIGH | recessive | LOW when bus dominant HIGH when bus recessive |
| Standby | HIGH | x (Note1) | biased to ground | follows BUS when wake-up detected HIGH when no wake-up detected |
| Off | x | x | High-Z state | High-Z state |

Note1: 'x' = don't care.

9.1.1 Normal mode

A LOW level on pin STB selects Normal mode, provided the supply voltage on pin V_{CC} is above the standby undervoltage detection threshold, $V_{UVD(STB)(VCC)}$. Additionally, for the UMCAN1472V variant, V_{IO} must be above the switch-off undervoltage detection threshold $V_{UVD(SWOFF)VIO}$.

In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 8-1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data on pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible EME. In order to support high bit rates, especially in CAN FD systems, the Signal Improvement function largely eliminates topology-related reflections and impedance mismatches. In recessive state, the output voltage on the bus pins is $V_{CC}/2$.

9.1.2 Standby mode

A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. In Standby mode, the bus lines are biased to ground to minimize system supply current. The low-power receiver is supplied from V_{IO} and can detect CAN bus activity even if V_{IO} is the only available supply voltage. Pin RXD follows the bus after a wake-up request has been detected. A transition to Normal mode is triggered when STB is forced LOW.

9.1.3 Off mode

The UMCAN1472 switches to Off mode from any mode when the supply voltage (on pin V_{IO} in the UMCAN1472V and V_{CC} in the UMCAN1472N) falls below the switch-off undervoltage threshold ($V_{UVD(SWOFF)VIO}$ OR $V_{UVD(SWOFF)VCC}$). This is the default mode when the supply is first connected. In Off mode, the CAN pins and pin RXD are in a High-Z state.

9.1.4 Operating modes and gap-free operation

Gap-free operation guarantees defined behavior at all voltage levels. Supply voltage-to-operating mode mapping is detailed in Figure 9-1.

| UMCAN1472V | | | | UMCAN1472N | |
|----------------------|---|--|---|---|---|
| Voltage range on VCC | 5.5 V - 7V (Note 1) | off | Fully functional or Off (Note 2, 3, 4) | Fully functional (Note 2, 3) | Fully functional (Note 2, 3) |
| | V _{CC} operating range (4.5 V - 5.5 V) | | Fully functional and characteristics guaranteed (Note 2, 5) | Fully functional and characteristics guaranteed (Note 2, 5) | |
| | V _{UVD(STB)VCC} range (Note6) | | Fully functional or Standby or Off (Note 2, 4) | Fully functional or Standby (Note 2, 4) | Fully functional or Standby (Note 2, 4) |
| | -0.3 V - 3 V | | Standby or Off (Note 4) | Standby | Standby |
| -0.3 V - 1.3 V | | V _{UVD(SWOFF)VIO} range (Note6) | | V _{IO} operating range (2.5 V - 5.5 V) | |
| 5.5 V - 7V (Note 1) | | Voltage range on VIO | | | |

Figure 9-1. Supply voltage ranges and gap-free operation

Note 1: Maximum voltage should never exceed 7 V.

Note 2: Target transceiver functionality as described in this datasheet is applicable.

Note 3: Prolonged operation of the device outside the operating range may impact reliability over lifetime. Returning to the operating range, datasheet characteristics are guaranteed provided the AMR has not been exceeded.

Note 4: For a given value of V_{IO}, a specific device will be in a single defined state determined by its undervoltage detection thresholds (V_{UVD(STB)VCC} and V_{UVD(SWOFF)VIO}). The actual thresholds can vary between devices (within the ranges specified in this datasheet). To guarantee the device will be in a specific state, V_{IO} and V_{CC} must be either above the maximum or below the minimum thresholds specified for these undervoltage detection ranges.

Note 5: Datasheet characteristics are guaranteed within the V_{CC} and V_{IO} operating ranges. Exceptions are described in the Static and Dynamic characteristics tables.

Note 6: The following applies to the UMCAN1472:

- If both V_{CC} and V_{IO} are above the undervoltage threshold, the device is fully functional.
- If V_{CC} is below and V_{IO} above the undervoltage threshold, the device is in Standby mode.
- If V_{IO} is below the undervoltage threshold, the device is in Off mode, regardless of V_{CC}.

9.2 Remote wake-up (via the CAN bus)

The UMCAN1472 wakes up from Standby mode when a dedicated wake-up pattern (specified in ISO 11898-2:2024) is detected on the bus. This filtering helps avoid spurious wake-up events. A spurious wake-up sequence could be triggered by, for example, a dominant clamped bus or by dominant phases due to noise or spikes on the bus.

The wake-up pattern consists of:

- a dominant phase of at least $t_{WK(BUSDOM)}$ followed by
- a recessive phase of at least $t_{WK(BUSREC)}$ followed by
- a dominant phase of at least $t_{WK(BUSDOM)}$

Dominant or recessive bits between the above mentioned phases that are shorter than $t_{WK(BUSDOM)}$ and $t_{WK(BUSREC)}$ respectively are ignored.

The complete dominant-recessive-dominant pattern must be received within $t_{TO(WK)BUS}$ to be recognized as a valid wake-up pattern. Otherwise, the internal wake-up logic is reset. The complete wake-up pattern will then need to be retransmitted to trigger a wake-up event. Pin RXD remains HIGH until the wake-up event has been triggered.

After a wake-up sequence has been detected, the UMCAN1472 will remain in Standby mode with the bus signals reflected on RXD after $t_{STARTUP(RXD)}$. Note that dominant or recessive phases lasting less than $t_{FLTR(WK)BUS}$ will not be detected by the low-power differential receiver and will not be reflected on RXD in Standby mode.

A wake-up event is not flagged on RXD if any of the following events occurs while a valid wake-up pattern is being received:

- The device switches to Normal mode
- The complete wake-up pattern was not received within $t_{TO(WK)BUS}$
- A V_{CC} or V_{IO} undervoltage is detected ($V_{CC} < V_{UVD(SWOFF)VCC}$ or $V_{IO} < V_{UVD(SWOFF)VIO}$; see 9.3.3)

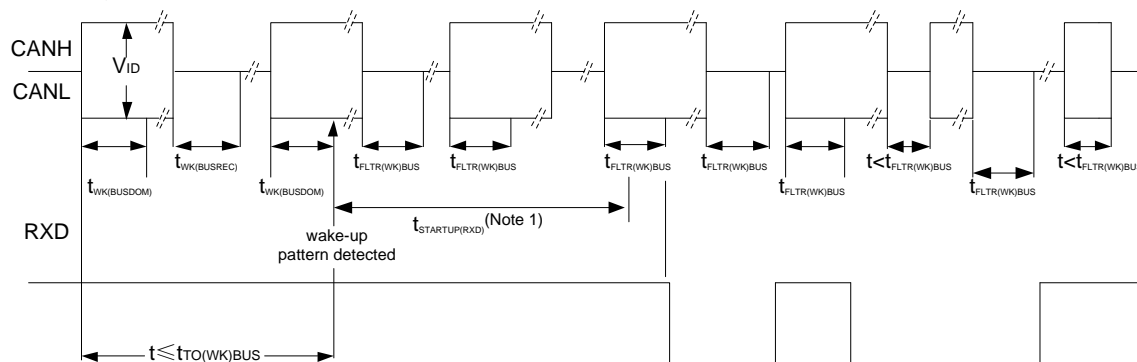


Figure 9-2. Wake-up Timing

Note 1: During $t_{STARTUP(RXD)}$, the low-power receiver is on but pin RXD is not active (i.e. HIGH/recessive). The first dominant pulse of width $\geq t_{FLTR(WK)BUS}$ that ends after $t_{STARTUP(RXD)}$ will trigger RXD to go LOW/dominant.

9.3 Fail-safe features

9.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on this pin persists for longer than $t_{TO(DOM)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

9.3.2 Internal biasing of TXD and STB input pins

Pins TXD and STB have internal pull-ups to V_{CC} (V_{IO} for variants with a V_{IO} pin) to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize supply current.

9.3.3 Undervoltage detection on pins V_{CC} and V_{IO}

If V_{CC} drops below the standby undervoltage detection level, $V_{UVD(STB)VCC}$, the transceiver switches to Standby mode. The logic state of pin STB is ignored until V_{CC} has recovered.

In versions with a V_{IO} pin, if V_{IO} drops below the switch-off undervoltage detection level ($V_{UVD(SWOFF)VIO}$), the transceiver switches off and disengages from the bus (High-Z) until V_{IO} has recovered.

In versions without a V_{IO} pin, if V_{CC} drops below the switch-off undervoltage detection level ($V_{UVD(SWOFF)VCC}$), the transceiver switches off and disengages from the bus (High-Z) until V_{CC} has recovered.

9.3.4 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the virtual junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, both output drivers are disabled. When the virtual junction temperature drops below $T_{J(SD)}$ again, the output drivers recover once TXD has been reset to HIGH. Including the TXD condition prevents output driver oscillation due to small variations in temperature.

9.3.5 VIO supply pin (UMCAN1472VS8 and UMCAN1472VDA variants)

Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver in the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC} .

For variants of the UMCAN1472 without a V_{IO} pin, all circuitry is connected to V_{CC} (pin 5 is not bonded). The signal levels of pins TXD, RXD and STB are then compatible with 5 V microcontrollers. This allows the device to interface with both 3.3 V and 5 V-supplied microcontrollers, provided the microcontroller I/Os are 5 V tolerant.

9.4 Signal Improvement

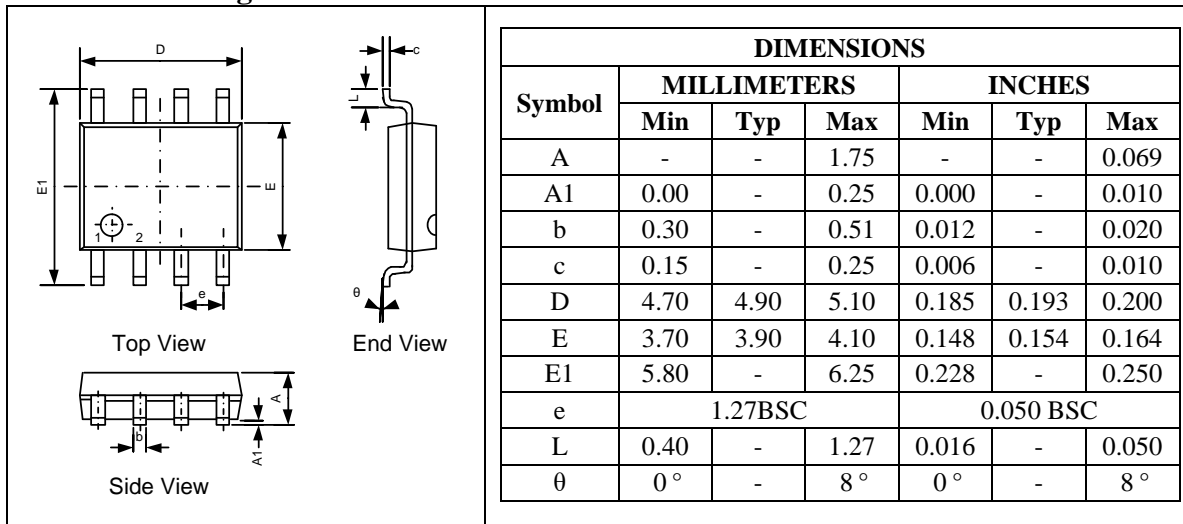
Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.

Recessive-to-dominant signal edge is usually clean as it is strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is $\approx 50 \Omega$ and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to $\approx 60 \text{ k}\Omega$ and signal reflected back experiences impedance mismatch which causes ringing. The UMCAN1472 resolves this issue by TX-based Signal improvement capability (SIC). The device continues to drive the bus recessive until $t_{SIC(TXD)BASE}$ so that reflections die down and recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low ($\approx 100 \Omega$). After this phase is over and device goes to passive recessive phase, driver output impedance goes to high-Z. This phenomenon is explained at Figure 7-5.

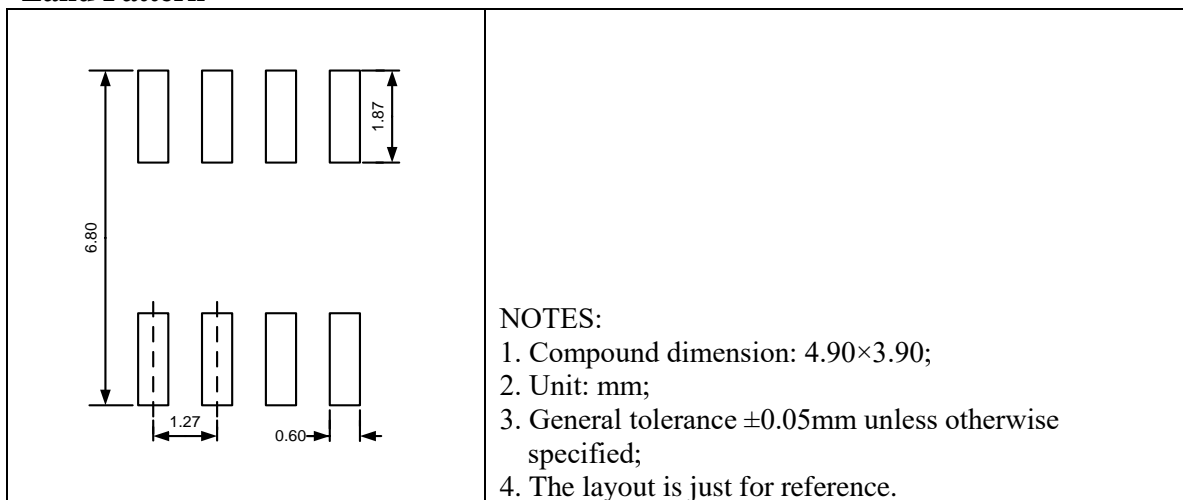
Package Information

SOP8

Outline Drawing

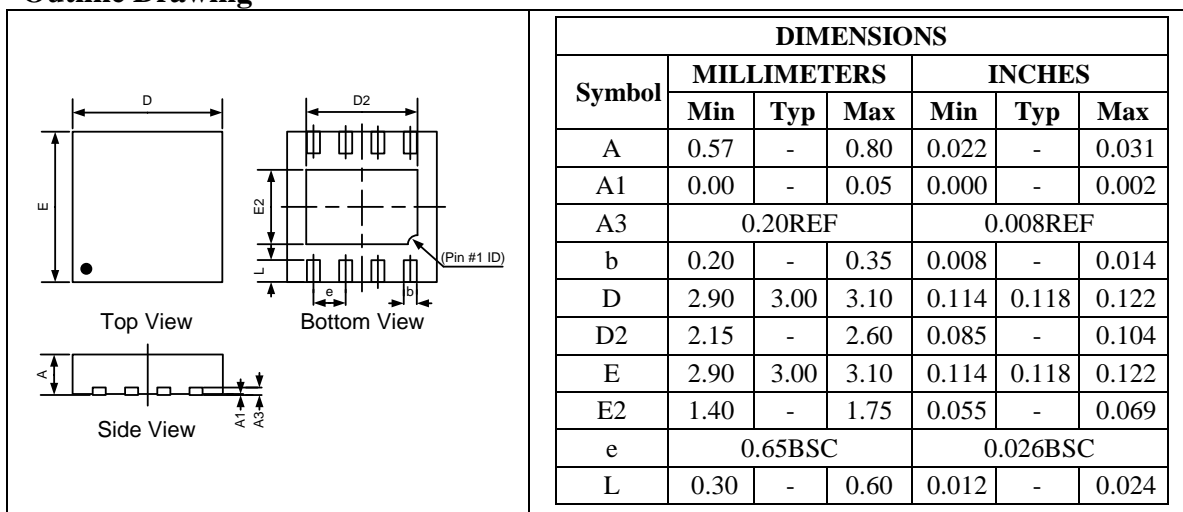


Land Pattern

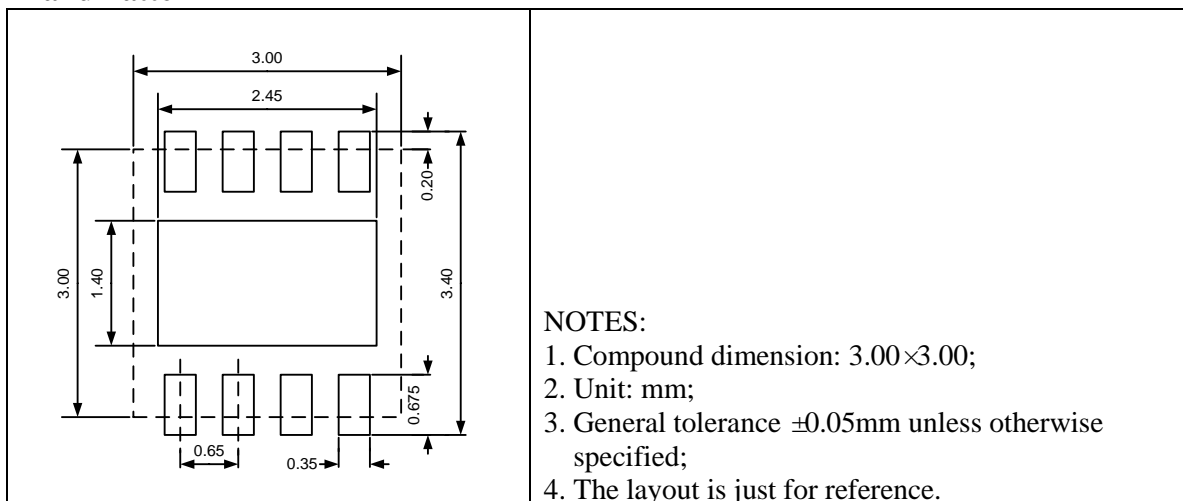


DFN8 3.0×3.0

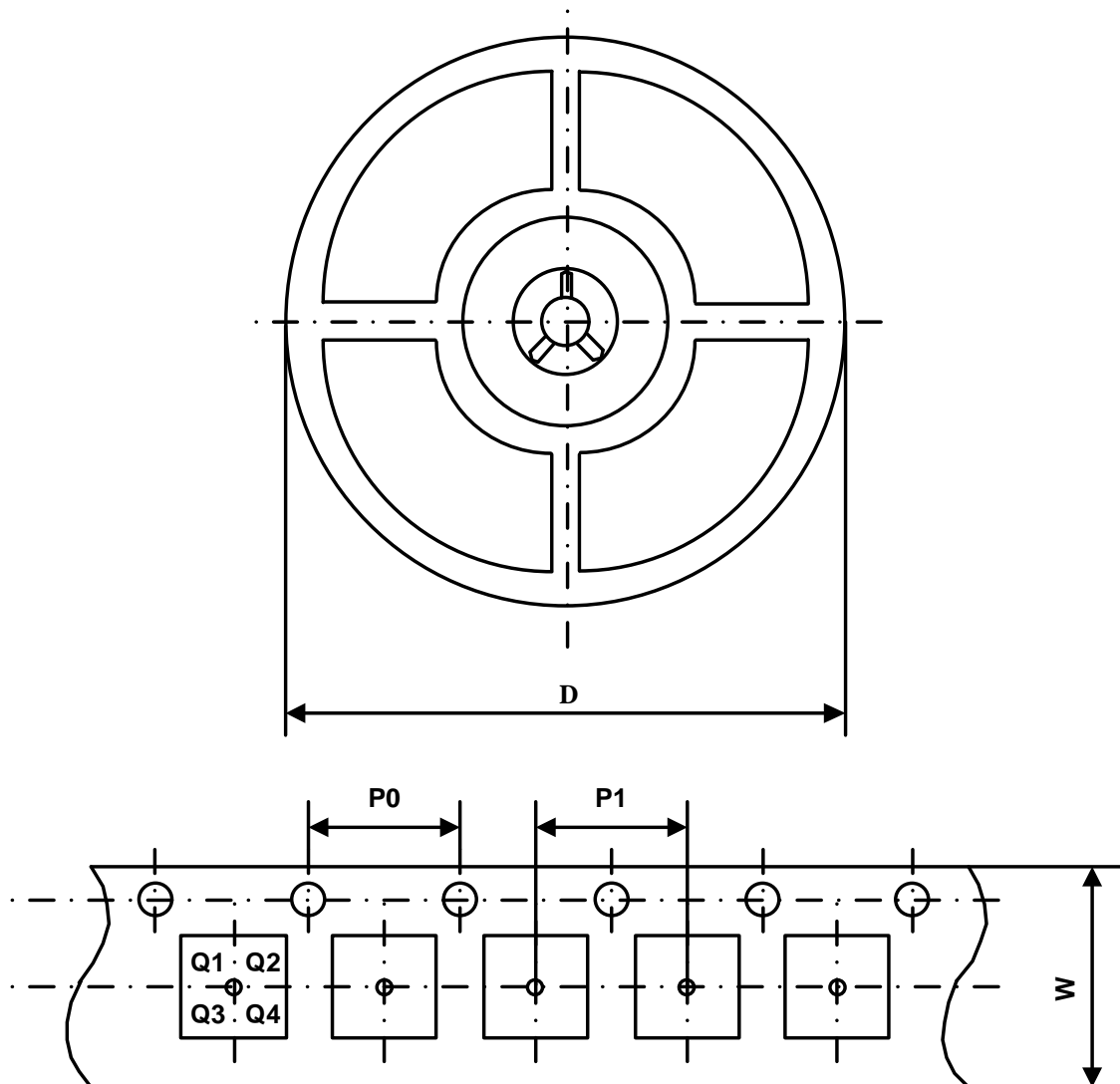
Outline Drawing



Land Pattern



Packing Information



| Part Number | Package Type | Carrier Width (W) | Pitch (P0) | Pitch (P1) | Reel Size (D) | PIN 1 Quadrant |
|--------------|--------------|-------------------|------------|------------|---------------|----------------|
| UMCAN1472VS8 | SOP8 | 12 mm | 4 mm | 8 mm | 330 mm | Q1 |
| UMCAN1472VDA | DFN8 3.0×3.0 | 12 mm | 4 mm | 8 mm | 330 mm | Q1 |
| UMCAN1472NS8 | SOP8 | 12 mm | 4 mm | 8 mm | 330 mm | Q1 |
| UMCAN1472NDA | DFN8 3.0×3.0 | 12 mm | 4 mm | 8 mm | 330 mm | Q1 |

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