High-Speed CAN Transceiver with Signal Improvement Capability (SIC)

UMCAN1057SVS8 ***SOP8***
UMCAN1057SVDA ***DFN8 3.0×3.0***

1 Description

The UMCAN1057S is a high-speed CAN transceiver that provides an interface between a Controller Area Network (CAN) protocol controller and the physical two-wire CAN bus. The transceiver is designed for high-speed CAN applications in the automotive industry, providing differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. The UMCAN1057S offers improved ElectroMagnetic Compatibility (EMC) and ElectroStatic Discharge (ESD) performance, and also features:

• Ideal passive behavior to the CAN bus when the supply voltage is off.
• Variants with a V_{IO} pin allows for direct interfacing with 3.3 V and 5 V supplied microcontrollers.

The UMCAN1057S implements the CAN physical layer as defined in ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5. The UMCAN1057S includes CAN signal improvement capability (SIC), as defined in ISO 11898-2:2024 parameter set C. CAN signal improvement significantly reduces signal ringing in a network, allowing reliable CAN FD communication to function in larger topologies. In addition, the UMCAN1057S features a much tighter bit timing symmetry performance to enable CAN FD communication up to 8 Mbit/s. These features make the UMCAN1057S an excellent choice for all types of HS-CAN networks, in nodes that do not require a standby mode with wake-up capability via the bus.

2 Applications

- Automotive Industry
- Industrial Control
- Wireless Infrastructure

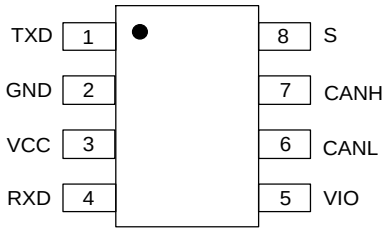
3 Features

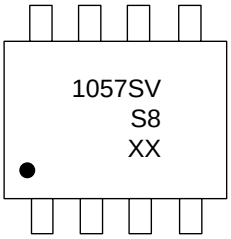
- ISO 11898-2:2024 and SAE J2284-1 to SAE J2284-5 compliant
- Implements CAN Signal Improvement Capability as defined in ISO 11898-2:2024 parameter set C to significantly reduce signal ringing effects in a network
- Tighter bit timing symmetry performance versus standard CAN FD transceivers allowing for data rates up to 8 Mbit/s
- Optimized for use in 12 V automotive systems
- Supply Voltage: 4.5V to 5.5V
- V_{IO} level shifting supports: 2.9V to 5.5V
- Transceiver disengages from the bus when not powered up (zero load)
- High ElectroStatic Discharge (ESD) handling capability on the bus pins
- Transmit Data (TXD) dominant time-out function
- Undervoltage detection on pins V_{CC} and V_{IO}
- Thermally protected

4 Ordering Information

Part Number	Marking Code	Package Type	Shipping Qty
UMCAN1057SVS8	1057SVS8	SOP8	3000pcs/13Inch Tape & Reel
UMCAN1057SVDA	1057SV	DFN8 3.0×3.0	3000pcs/13Inch Tape & Reel

5 Pin Configuration and Function





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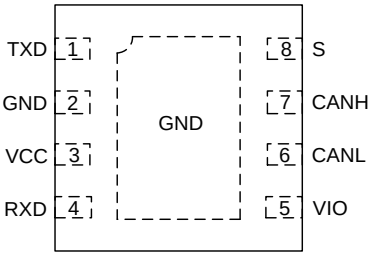
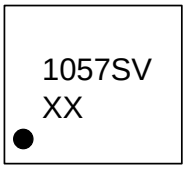
SOP8





XX: Week Code
UMCAN1057SVDA
DFN8 3.0×3.0

Table 5-1. Pin Functions

Pin No.	Symbol	Description
1	TXD	Transmit data input
2	GND	Ground (Note1)
3	VCC	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	V_{IO}	Supply voltage for I/O level adapter;
6	CANL	Low-level CAN bus line
7	CANH	High-level CAN bus line
8	S	Silent mode control input

Note 1: DFN8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

6 Specifications

6.1 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Bus supply voltage		4.5		5.5	V
V_{IO}	Supply voltage I/O level shifter		2.9		5.5	V
T_A	Operating ambient temperature		-40		125	℃

6.2 Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_I	Voltage range on CANH, CANL		-40		+40	V
	Voltage range on V_{CC}, V_{IO}		-0.3		+7	V
	Voltage range on any other pin	Note 3	-0.3		V_{IO}+0.3	V
V_{DIF}	Voltage range between CANH and CANL		-40		+40	V
V_{trt}	Transient voltage on CANH, CANL pins (Note 4)	pulse 1	-100			V
		pulse 2a			+75	V
		pulse 3a	-150			V
		pulse 3b			+100	V
V_{ESD}	Contact discharge, per IEC 61000-4-2	Bus pins		±10		kV
	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
	Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002	All pins		±2		kV
I_{LU}	Latch up, per JEDEC JESD78	Class II		200		mA
T_{VJ}	Virtual junction temperature		-40		150	℃
T_{STG}	Storage temperature		-55		150	℃

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
Note 2: All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
Note 3: Maximum voltage should never exceed 7 V.
Note 4: Verified by an external test house according to IEC TS 62228, Section 4.2.4; parameters for standard pulses defined in ISO 7637.

6.3 Electrical Characteristics (Static) (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply; pin VCC						
V_{CC}	Supply voltage		4.5		5.5	V
V_{UVD}	Undervoltage detection voltage on pin VCC		3.5	4	4.3	V
I_{CC}	Supply current	Normal mode; TXD = 0 V; short circuit on bus lines; -3V < (CANH=CANL)<18V		80	110	mA
		Normal mode; TXD = V_{IO}		1.6	5	mA
		Normal mode; TXD = 0 V	20	45	60	mA
		Silent mode; TXD = V_{IO}	0.1		2	mA
I/O level adapter supply; pin VIO						
V_{IO}	Supply voltage on pin VIO		2.9		5.5	V
V_{UVD}	Undervoltage detection voltage on pin VIO		2.1		2.8	V
I_{IO}	Supply current on pin VIO	Normal mode; TXD = 0V		165	300	uA
		Normal mode; TXD = V_{IO}		15	30	uA
		Silent mode		15	30	uA
Mode control inputs; pins S						
V_{IH}	High-level input voltage		0.7V_{IO}			V
V_{IL}	Low-level input voltage				0.3V_{IO}	V
I_{IH}	High-level input current	V_{IN} = V_{IO}	1		10	uA
I_{IL}	Low-level input current	V_{IN} = 0 V	-1		-1	uA

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN transmit data input; pin TXD						
V_{IH}	High-level input voltage		$0.7V_{IO}$			V
V_{IL}	Low-level input voltage				$0.3V_{IO}$	V
I_{IH}	High-level input current	$V_{IN} = V_{IO}$	-5		5	uA
I_{IL}	Low-level input current	V_{IN} = 0 V	-270	-100	-30	uA
C_I	Input capacitance			5	10	pF
CAN receive data output; pin RXD						
I_{OH}	High-level output current	RXD = V_{IO} - 0.4 V	-9	-1.5		mA
I_{OL}	Low-level output current	RXD = 0.4 V		1.5	12	mA
Driver						
$V_{O(DOM)}$	Dominant output voltage	TXD = 0 V; t < $t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω; pin CANH	2.75	3.5	4.5	V
		TXD = 0 V; t < $t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω; pin CANL	0.5	1.5	2.25	V
$V_{OD(DOM)}$	Dominant differential output voltage	TXD = 0 V; t < $t_{TO(DOM)TXD}$; 50 Ω ≤ R_L ≤ 65 Ω;	1.5		3	V
		TXD = 0 V; t < $t_{TO(DOM)TXD}$; 45 Ω ≤ R_L ≤ 70 Ω;	1.4		3.3	V
		TXD = 0 V; t < $t_{TO(DOM)TXD}$; R_L = 2240 Ω;	1.5		5	V
$V_{O(REC)}$	Recessive output voltage	Normal or silent mode; TXD = V_{IO}; R_L = open	2	$0.5V_{CC}$	3	V
$V_{OD(REC)}$	Recessive differential output voltage	Normal or silent mode; TXD = V_{IO}; R_L = open	-50		50	mV
$V_{SYM(DOM)}$	Dominant output voltage symmetry, V_{CC}-CANH-CANL	TXD = 0 V; t < $t_{TO(DOM)TXD}$; R_L = 60 Ω	-400		400	mV

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{SYM(TX)}$	Transmitter output voltage symmetry, (CANH+CANL)/V_{CC}	TXD = 250 kHz, 1 MHz, 2.5MHz; R_L = 60 Ω; C_{SPLIT} = 4.7 nF	0.9V_{CC}		1.1V_{CC}	V
$V_{CM(STEP)}$	Common mode voltage step	See figure 7-4	-150		150	mV
$V_{CM(PP)}$	Peak-to-peak common mode voltage	See figure 7-4	-400		400	mV
$I_{OS(DOM)}$	Dominant short-circuit output current	TXD = 0 V; t < $t_{TO(DOM)TXD}$; V_{CC} = 5 V; CANH = -15 V to 40 V; pin CANH	-100	-70		mA
		TXD = 0 V; t < $t_{TO(DOM)TXD}$; V_{CC} = 5 V; CANL = -15 V to 40 V; pin CANL		70	100	mA
$I_{OS(REC)}$	Recessive short-circuit output current	Normal mode; TXD = V_{IO}; –27 V≤ CANH = CANL ≤ 32 V	-5		5	mA
Receiver						
V_{TH}	Differential receiver threshold voltage	Normal or silent mode; -15 V≤ CANH, CANL ≤ 15 V	0.5		0.9	V
$V_{ID(REC)}$	Receiver recessive voltage	Normal or silent mode; -15 V ≤ CANH, CANL ≤ 15 V (Note2)	-4		0.5	V
$V_{ID(DOM)}$	Receiver recessive voltage	Normal or silent mode; -15 V ≤ CANH, CANL ≤ 15 V (Note2)	0.9		9	V
V_{HYS}	Differential receiver hysteresis voltage	Normal or silent mode; -15 V ≤ CANH, CANL ≤ 15 V	50		300	mV
$I_{LKG(PD)}$	Unpowered Leakage current	V_{CC} = V_{IO} = 0 V or shorted to GND via 47 kΩ; CANH = CANL = 5 V	-5		18	uA
R_I	Input resistance	-2 V ≤ CANH, CANL ≤ 7 V (Note2)	15	30	40	kΩ
ΔR_I	Input resistance deviation, [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	0 V ≤ CANH, CANL ≤ 5 V (Note2)	-3		3	%

6.3 Electrical Characteristics (Static)---continued (Note 1)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; All voltages are defined with respect to ground; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
R_{ID}	Differential input resistance	-2 V ≤ CANH, CANL ≤ 7 V (Note3)	30	60	80	kΩ
C_{IN}	Common-mode input capacitance to ground	Note3			20	pF
C_{ID}	Differential input capacitance	Note3			10	pF
Thermal Protection						
$T_{J(SD)}$	Shutdown junction temperature	Note3		185		℃

Note 1: V_{IO} = V_{CC} in non-VIO product variants.
Note 2: Not tested in production; guaranteed by design.

6.4 Electrical Characteristics (Dynamic)

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; all voltages are defined with respect to ground.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
CAN timing characteristics according to ISO 11898-2:2024; see Figure 7-1 and Figure 7-3						
$t_{D(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	Normal mode; R_L = 60 Ω, C_L = 100 pF			255	ns
$t_{D(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	Normal mode; R_L = 60 Ω, C_L = 100 pF			255	ns
CAN timing characteristics according to ISO 11898-2:2024; VCC = 4.75 V to 5.25 V; see Figure 7-1, Figure 7-3 and Figure 7-5;						
$t_{D(TXD-BUSDOM)}$	Delay time from TXD to bus dominant	Normal mode; R_L = 60 Ω, C_L = 100 pF			80	ns
$t_{D(TXD-BUSREC)}$	Delay time from TXD to bus recessive	Normal mode; R_L = 60 Ω, C_L = 100 pF			80	ns
$t_{D(BUSDOM-RXD)}$	Delay time from bus dominant to RXD	Normal mode; $C_{L(RXD)}$ = 15 pF			110	ns
$t_{D(BUSREC-RXD)}$	Delay time from bus recessive to RXD	Normal mode; $C_{L(RXD)}$ = 15 pF			110	ns
$t_{D(TXDL-RXDL)}$	Delay time from TXD LOW to RXD LOW	Normal mode; R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF			190	ns
$t_{D(TXDH-RXDH)}$	Delay time from TXD HIGH to RXD HIGH	Normal mode; R_L = 60 Ω, C_L = 100 pF, $C_{L(RXD)}$ = 15 pF			190	ns
$t_{SIC(TXD)BASE}$	delay time from TXD to bus active recessive end	Normal mode (Note 1)	355		480	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set C($t_{BIT(TXD)}$ ≥125 ns, up to 8 Mbit/s; V_{CC} = 4.75 V to 5.25 V; see Figure 7-1 and Figure 7-3); (Note 2)						
$\Delta t_{BIT(BUS)}$	Transmitted recessive bit width deviation	$\Delta t_{BIT(BUS)} = t_{BIT(BUS)} - t_{BIT(TXD)}$	-10		10	ns
Δt_{REC}	Receiver timing symmetry	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-20		15	ns
$\Delta t_{BIT(RXD)}$	Received recessive bit width deviation	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-30		20	ns

6.4 Electrical Characteristics (Dynamic) ---continued

T_J = -40℃ to +150℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.9V to 5.5V; R_L = 60Ω; C_L = 100pF unless otherwise specified; all voltages are defined with respect to ground.

CAN FD timing characteristics according to ISO 11898-2:2024 parameter set B ($t_{BIT(TXD)}$) ≥ 200 ns, up to 5 Mbit/s); See figure 7-1 and figure 7-3						
$\Delta t_{BIT(BUS)}$	Transmitted recessive bit width deviation	$\Delta t_{BIT(BUS)} = t_{BIT(BUS)} - t_{BIT(TXD)}$	-45		10	ns
Δt_{REC}	Receiver timing symmetry	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-45		15	ns
$\Delta t_{BIT(RXD)}$	Received recessive bit width deviation	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-80		20	ns
CAN FD timing characteristics according to ISO 11898-2:2024 parameter set A ($t_{BIT(TXD)}$) ≥ 500 ns, up to 2 Mbit/s); See figure 7-1 and figure 7-3						
$\Delta t_{BIT(BUS)}$	Transmitted recessive bit width deviation	$\Delta t_{BIT(BUS)} = t_{BIT(BUS)} - t_{BIT(TXD)}$	-65		30	ns
Δt_{REC}	Receiver timing symmetry	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(BUS)}$	-65		40	ns
$\Delta t_{BIT(RXD)}$	Received recessive bit width deviation	$\Delta t_{REC} = t_{BIT(RXD)} - t_{BIT(TXD)}$	-100		50	ns
Dominant time-out time; pin TXD; (Note 3)						
$t_{TO(DOM)TXD}$	TXD dominant time-out time	Normal mode; TXD = 0V	0.8	2.6	6.5	ms

Note 1: Not tested in production; guaranteed by design.
Note 2: Compliance with parameter set C requirements implies compliance for parameter sets A ($t_{BIT(TXD)}$) ≥ 500 ns, up to 2 Mbit/s) and B ($t_{BIT(TXD)}$) ≥ 200 ns, up to 5 Mbit/s).
Note 3: Time-out occurs between the min and max values. Time-out is guaranteed not to occur below the min value; time-out is guaranteed to occur above the max value.

7 Parameter Measurement Information

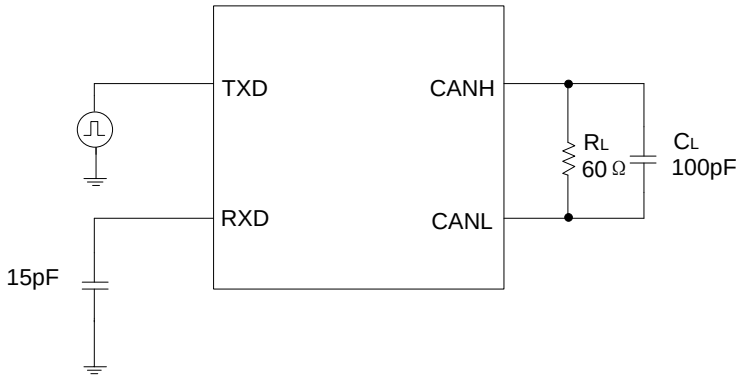


Figure 7-1. CAN transceiver timing test circuit

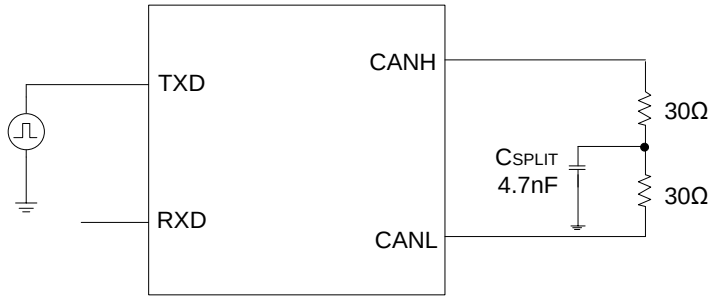


Figure 7-2. Test circuit for measuring transceiver transmitter driver symmetry

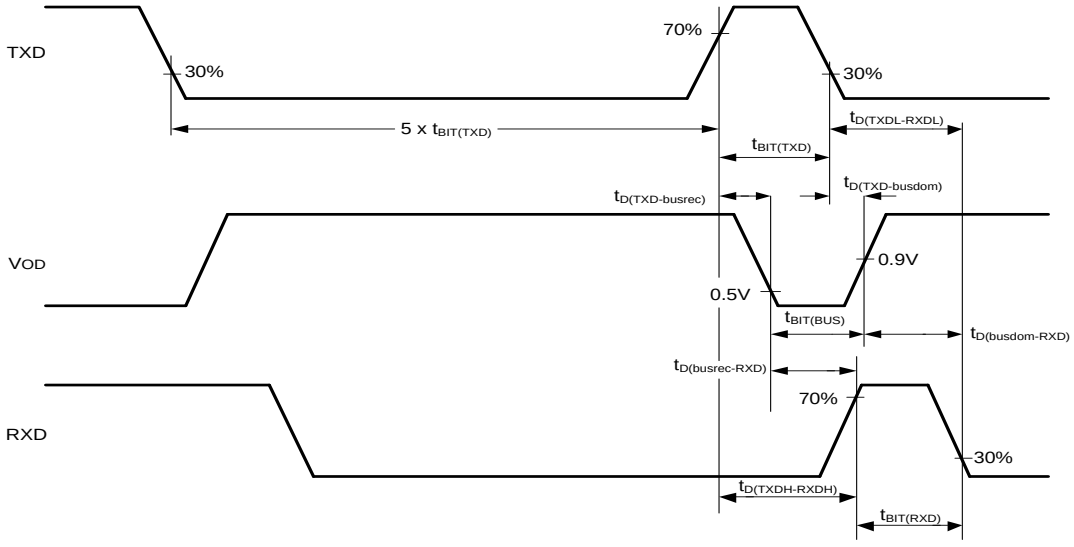


Figure 7-3. CAN FD timing definitions according to ISO 11898-2:2024

7 Parameter Measurement Information (continued)

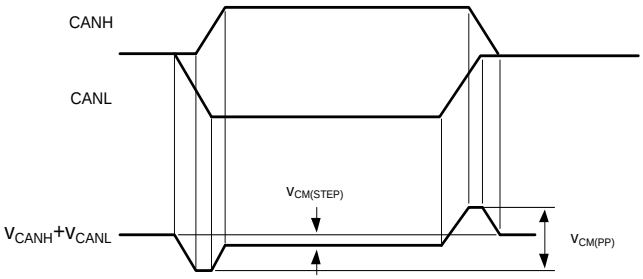


Figure 7-4. CAN bus common-mode voltage according to SAE 1939-14

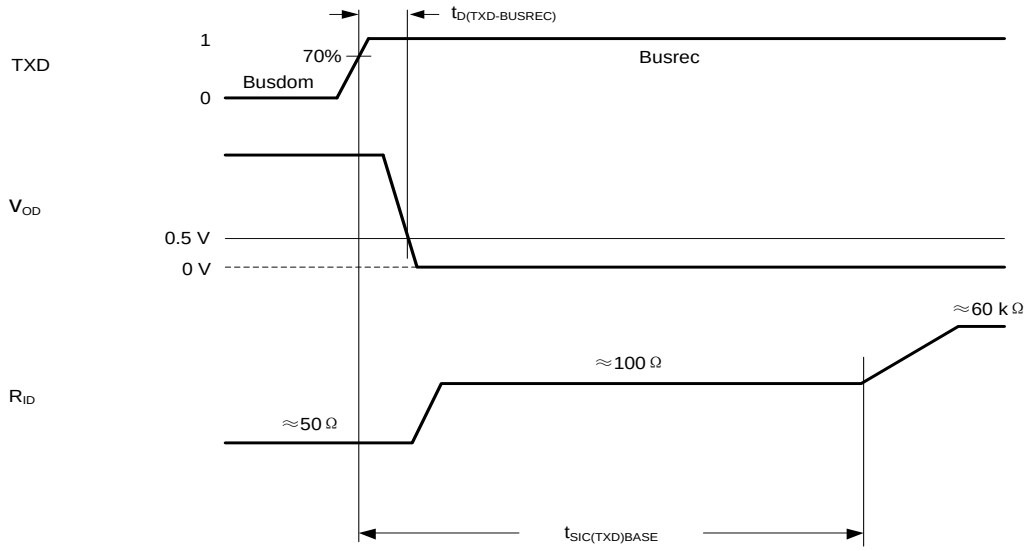


Figure 7-5. UMCAN1057S transmitter impedance and timing diagram for dominant-to-passive recessive transition

8 Block diagram

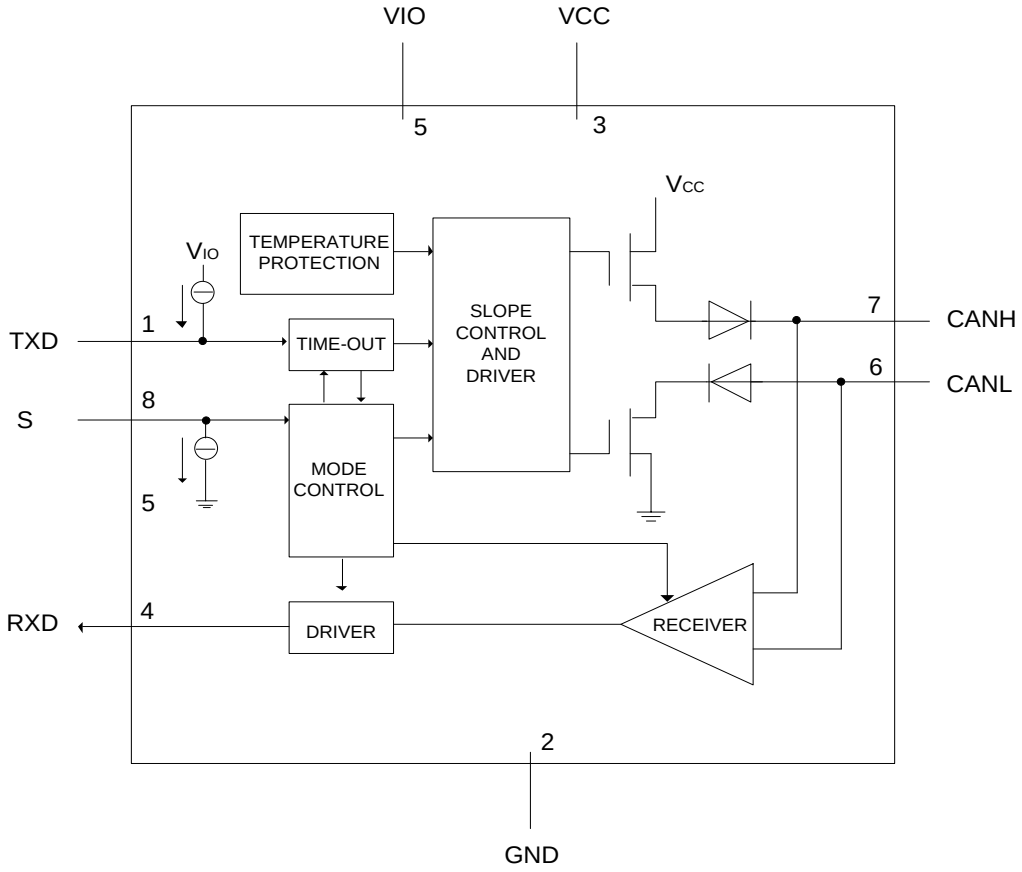


Figure 8-1. Block diagram

9 Detailed Description

9.1 Functional Description

The UMCAN1057S is a high-speed CAN stand-alone transceiver with Silent mode. It combines the functionality of transceiver with improved EMC and ESD handling capability. Improved slope control and high DC handling capability on the bus pins provides additional application flexibility. The UMCAN1057S allows for direct interfacing to microcontrollers with supply voltages down to 3.3 V.

9.2 Operating modes

The UMCAN1057S supports two operating modes, Normal and Silent, which are selected via pin S. See Table 1 for a description of the operating modes under normal supply conditions.

Table 9-1. Operating modes

Mode	Inputs		Outputs	
	Pin S	**Pin TXD**	**CAN driver**	**Pin RXD**
Normal	LOW	LOW	dominant	Active (Note1)
	LOW	HIGH	recessive	Active (Note1)
Silent	HIGH	X (Note2)	recessive	Active (Note1)

Note1: LOW if the CAN bus is dominant, HIGH if the CAN bus is recessive.
Note2: 'X' = Don't care.

9.2.1 Normal mode

A LOW level on pin S selects Normal mode. In this mode, the transceiver is able to transmit and receive data via the bus lines CANH and CANL (see Figure 8-1 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are optimized in a way that guarantees the lowest possible ElectroMagnetic Emission (EME).

9.2.2 Silent mode

A HIGH level on pin S selects Silent mode. In Silent mode the transmitter is disabled, releasing the bus pins to recessive state. All other IC functions, including the receiver, continue to operate as in Normal mode. Silent mode can be used to prevent a faulty CAN controller from disrupting all network communications.

9.3 Fail-Safe Features

9.3.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{TO(DOM)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

9.3.2 Internal biasing of TXD and S input pins

Pin TXD has an internal pull-up to V_{IO} and pins S has internal pull-downs to GND. This ensures a safe, defined state in case one or more of these pins is left floating.

9.3.3 Undervoltage detection on pins V_{IO}

Should V_{IO} drop below the undervoltage detection levels ($V_{UVD(VIO)}$), the transceiver will switch off and disengage from the bus (zero load) until V_{IO} have recovered.

9.3.4 Over temperature protection

The output drivers are protected against over temperature conditions. If the operating junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, the output drivers will be disabled until the operating junction temperature falls below $T_{J(SD)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

9.3.5 V_{IO} supply pin

Pin V_{IO} should be connected to the microcontroller supply voltage. This will adjust the signal levels of pins TXD, RXD and S to the I/O levels of the microcontroller.

9.4 Signal Improvement

Signal improvement is an additional capability added to CAN FD transceiver that enhances the maximum data rate achievable in complex star topologies by minimizing signal ringing. Signal ringing is the result of reflections caused by impedance mismatch at various points in a CAN network due to the nodes that act as stubs.
Recessive-to-dominant signal edge is usually clean as it is strongly driven by the transmitter. Transmitter output impedance of CAN transceiver is ≈ 50 Ω and matches to the network characteristic impedance. For a regular CAN FD transceiver, dominant-to-recessive edge is when the driver output impedance goes to ≈ 60 kΩ and signal reflected back experiences impedance mismatch which causes ringing. UMCAN1057S resolves this issue by TX-based Signal improvement capability (SIC). The device continues to drive the bus recessive until $t_{SIC(TXD)BASE}$ so that reflections die down and recessive bit is clean at sampling point. In the active recessive phase, transmitter output impedance is low (≈ 100 Ω). After this phase is over and device goes to passive recessive phase, driver output impedance goes to High-Z. This phenomenon is explained at Figure 7-5.

10 Application Information

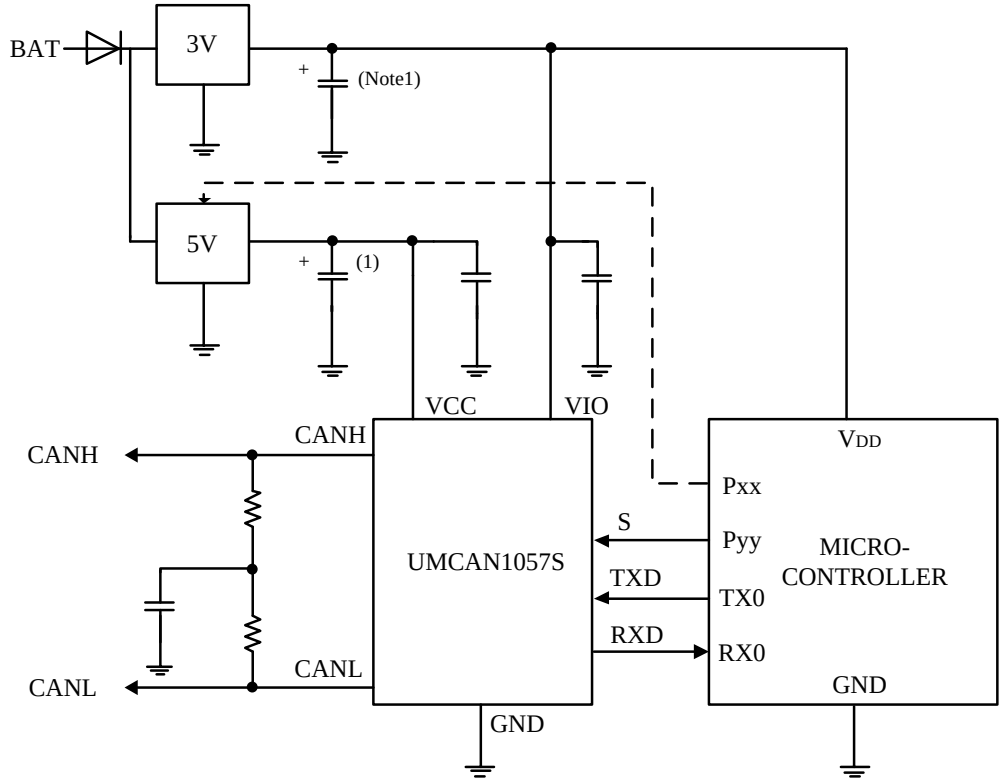


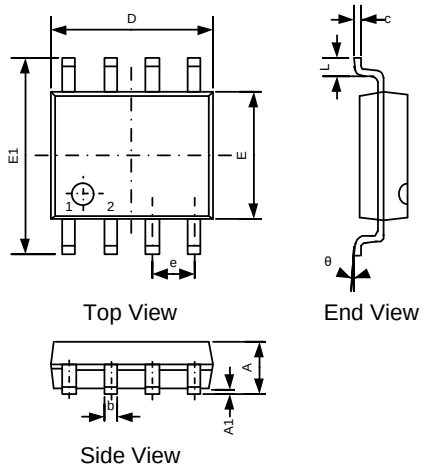
Figure 10-1. Typical application of the UMCAN1057S

Note1: Optional, depends on regulator

Package Information

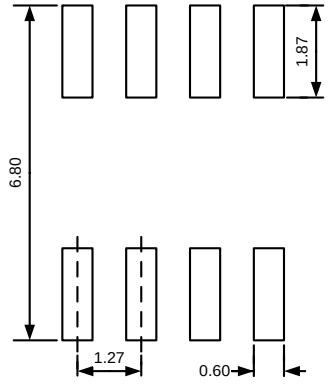
SOP8

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.75	-	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
b	0.30	-	0.51	0.012	-	0.020
c	0.15	-	0.25	0.006	-	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.70	3.90	4.10	0.148	0.154	0.164
E1	5.80	-	6.25	0.228	-	0.250
e	1.27BSC			0.050 BSC		
L	0.40	-	1.27	0.016	-	0.050
θ	0 °	-	8 °	0 °	-	8 °

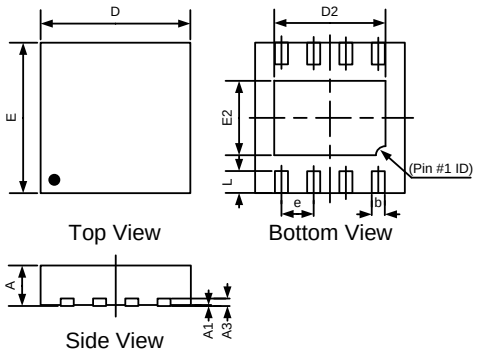
Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

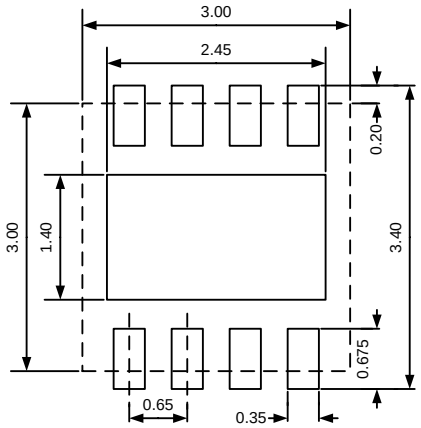
DFN8 3.0×3.0

Outline Drawing



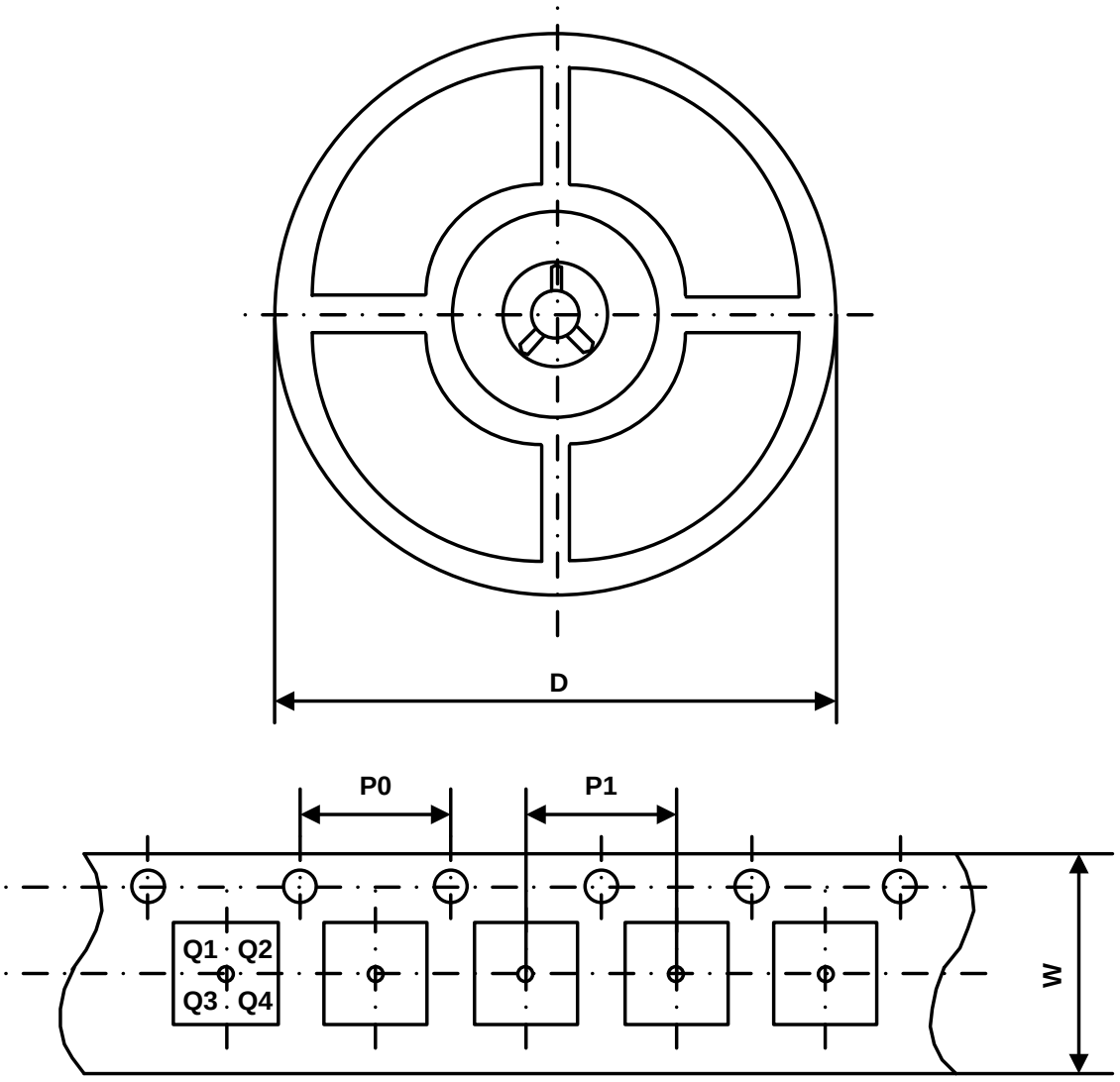
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.57	-	0.80	0.022	-	0.031
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20REF			0.008REF		
b	0.20	-	0.35	0.008	-	0.014
D	2.90	3.00	3.10	0.114	0.118	0.122
D2	2.15	-	2.60	0.085	-	0.104
E	2.90	3.00	3.10	0.114	0.118	0.122
E2	1.40	-	1.75	0.055	-	0.069
e	0.65BSC			0.026BSC		
L	0.30	-	0.60	0.012	-	0.024

Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMCAN1057SVS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMCAN1057SVDA	DFN8 3.0×3.0	12 mm	4 mm	8 mm	330 mm	Q1

GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.
All Union components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives. For more green compliance information, please visit:
https://www.union-ic.com/Quality.html

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