带手动复位输入的4引脚微处理器电压监测器

UM805/811/812 *SOT143*

描述

UM805/811/812是一款低功耗微处理器（μP）监控电路，用于监测微处理器和数字系统中的电源。当该器件与5V或3V供电电路配合使用时，无需外部元件，也不用进行调整，可实现非常可靠的低成本电路。

UM805/811/812仅执行单一功能：每当V_{CC}电源电压下降到预设阈值以下，它们都会输出复位信号，并在V_{CC}上升到复位阈值以上后将该信号保持输出状态至少140ms。此外，还可提供适合各种电源电压的复位阈值。

UM805有一个开漏输出，而UM811/812则有推挽输出。UM805的开漏低电平有效复位输出$\overline{RESET}$需要一个上拉电阻，该电阻可连接到高于V_{CC}的电压。UM805/811有一个低电平有效复位输出$\overline{RESET}$，而UM812有一个高电平有效复位输出RESET。复位比较器旨在忽略V_{CC}的快速瞬变，并确保在V_{CC}低至1V时，输出能够处于正确逻辑状态。

UM805/811/812具有低供电电流，因此非常适合用于便携式设备。这些器件采用4引脚SOT143封装。

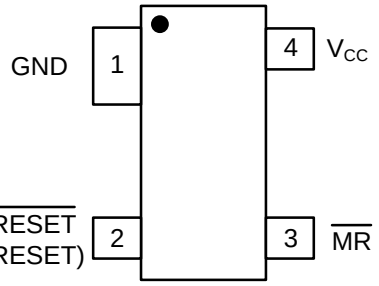
应用

- 计算机
- 控制器
- 便携式电池供电设备
- 智能仪表
- 精确的 μP 和 μC 电源监控

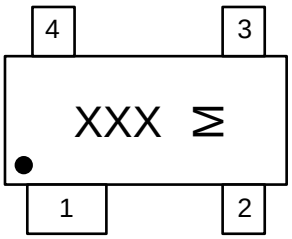
特性

- 无需外部元件
- 电源瞬变抗扰度
- 确保 V_{CC}=1V 时的正确逻辑输出
- 对 3V、3.3V 和 5V 电源进行精确电压监控
- 供电电流：2μA
- 最小上电复位脉冲宽度：140ms
- 工作温度范围内稳定可靠
- 有 3 种输出配置：
  低电平有效的开漏复位输出 $\overline{RESET}$ (UM805)
  低电平有效的推挽复位输出 $\overline{RESET}$ (UM811)
  高电平有效的推挽复位输出 RESET(UM812)
- 4 引脚 SOT143 封装
- 工作温度范围：-40℃ 至+85℃

Pin Configurations **Top View**



( ) are for UM812

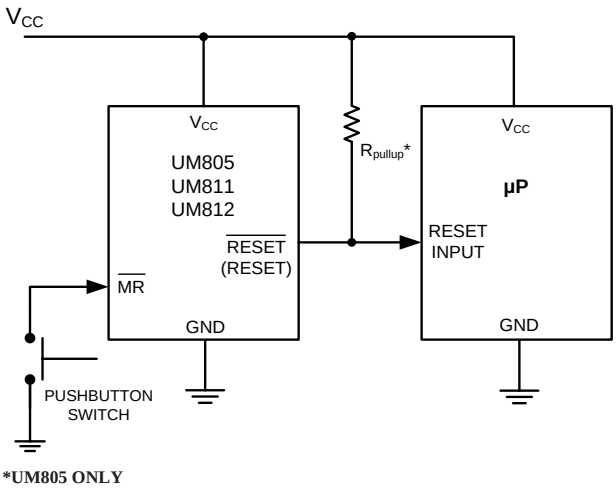


M: Month Code
UM805/811/812
SOT143

Ordering Information

UM8 XX Z P
XX: Output Type
=05 Open-Drain Active Low
=11 Push-Pull Active Low
=12 Push-Pull Active High
Z: Reset Threshold (V)
=L 4.63
=M 4.38
=J 4.00
=T 3.08
=S 2.93
=R 2.63
=Z 2.32
P: Package Type
=E SOT143

Typical Operating Circuit



***UM805 ONLY**
( ) are for UM812

Pin Description

Pin Number	Pin Name	Function
1	GND	Ground
2	$\overline{\text{RESET}}$ (UM805/811)	Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. It remains low for the Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated. **See Figure 1.** **UM811:** CMOS push-pull output (sources and sinks current). **UM805:** Open-drain, active low, NMOS output (sinks current only). Connect a pull-up resistor from $\overline{\text{RESET}}$ to any supply voltage up to 6V.
	RESET (UM812)	Active-High Reset Output. RESET remains high while V_{CC} is below the reset threshold or while $\overline{\text{MR}}$ is held low. RESET remains high for Reset Active Timeout Period (t_{RP}) after the reset conditions are terminated.
3	$\overline{\text{MR}}$	Manual Reset Input. A logic low on $\overline{\text{MR}}$ asserts reset. Reset remains asserted as long as $\overline{\text{MR}}$ is low and for 240ms after $\overline{\text{MR}}$ returns high. This active-low input has an internal 20kΩ pull-up resistor. It can be driven from a TTL or CMOS-logic line, or shorted to ground with a switch. Leave open if unused. **See Figure 2.**
4	V_{CC}	+5V, +3.3V or +3V Supply Voltage

Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.3 to +6.0	V
	RESET, $\overline{\text{RESET}}$ (Push-Pull)	-0.3 to (V_{CC}+0.3)	
	$\overline{\text{RESET}}$ (Open-Drain)	-0.3 to +6.0	
I_{CC}	Input Current, V_{CC}, $\overline{\text{MR}}$	20	mA
I_O	Output Current, RESET, $\overline{\text{RESET}}$	20	mA
P_D	Continuous Power Dissipation (Derate 4mW/℃ above 70℃)	320	mW
T_A	Operating Temperature Range	-40 to +85	℃
T_{STG}	Storage Temperature Range	-65 to +160	℃
	Lead Temperature (Soldering, 10s)	+300	℃

Note 1: Stresses beyond those listed under "Absolute maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC}=5V for L/M/J versions, V_{CC}=3.3V for T/S versions, V_{CC}=3V for R version, and V_{CC}=2.5V for Z version, T_A=-40℃ to +85℃, unless otherwise noted. Typical values are at T_A=+25℃.) (Note 2)

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range	T_A=0℃ to +70℃		1.0		5.5	V
I_{CC}	Supply Current				2.0	5.0	μA
V_{TH+}	Reset Threshold	L Version	T_A=+25℃	4.56	4.63	4.70	V
			T_A=-40℃ to +85℃	4.50		4.75	
		M Version	T_A=+25℃	4.31	4.38	4.45	
			T_A=-40℃ to +85℃	4.25		4.50	
		J Version	T_A=+25℃	3.93	4.00	4.06	
			T_A=-40℃ to +85℃	3.89		4.10	
		T Version	T_A=+25℃	3.04	3.08	3.11	
			T_A=-40℃ to +85℃	3.00		3.15	
		S Version	T_A=+25℃	2.89	2.93	2.96	
			T_A=-40℃ to +85℃	2.85		3.00	
		R Version	T_A=+25℃	2.59	2.63	2.66	
			T_A=-40℃ to +85℃	2.55		2.70	
		Z Version	T_A=+25℃	2.28	2.32	2.35	
			T_A=-40℃ to +85℃	2.25		2.38	
	Reset Threshold Tempco				150		ppm/℃
	V_{CC} to Reset Delay (Note 3)				10		μs
t_{RP}	Reset Active Timeout Period			140	240	560	ms
t_{MR}	$\overline{MR}$ Minimum Pulse Width			10			μs
	$\overline{MR}$ Glitch Immunity (Note 4)				100		ns
t_{MD}	$\overline{MR}$ to Reset Propagation Delay				0.5		μs
V_{IH}	$\overline{MR}$ Input Threshold	V_{CC}>$V_{TH(MAX)}$ UM805/811/812LE/ME/JE		2.3			V
V_{IL}						0.8	
V_{IH}		V_{CC}>$V_{TH(MAX)}$ UM805/811/812TE/SE/RE/ZE		0.7×V_{CC}			
V_{IL}						0.25×V_{CC}	
	$\overline{MR}$ Pull-Up Resistance			10	20	30	kΩ

Electrical Characteristics (Continued)

(V_{CC}=5V for L/M/J versions, V_{CC}=3.3V for T/S versions, V_{CC}=3V for R version, and V_{CC}=2.5V for Z version, T_A=-40℃ to +85℃, unless otherwise noted. Typical values are at T_A=+25℃.) (Note 2)

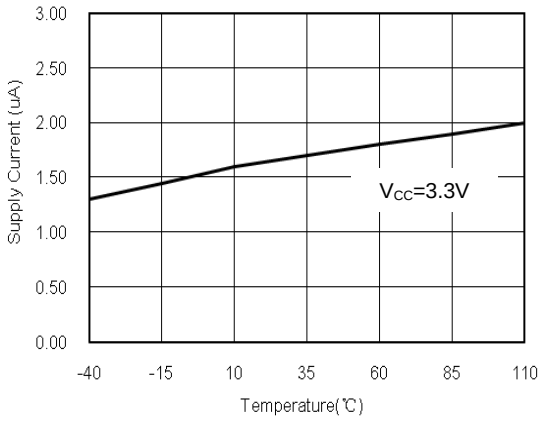
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	RESET Output Voltage	I_{SOURCE}=150μA, 1.8V<V_{CC}<$V_{TH(MIN)}$ UM812LE/ME/JE/TE/SE/RE/ZE	0.8×V_{CC}			V
V_{OL}		I_{SINK}=1.2mA UM812TE/SE/RE/ZE			0.3	
		I_{SINK}=3.2mA UM812LE/ME/JE			0.4	
V_{OH}	$\overline{RESET}$ Output Voltage	I_{SOURCE}=500μA, V_{CC}>$V_{TH(MAX)}$ UM811TE/SE/RE/ZE	0.8×V_{CC}			V
		I_{SOURCE}=800μA, V_{CC}>$V_{TH(MAX)}$ UM811LE/ME/JE	V_{CC}-1.5			
V_{OL}		I_{SINK}=1.2mA, V_{CC}=$V_{TH(MIN)}$ UM805/811TE/SE/RE/ZE			0.3	
		I_{SINK}=3.2mA, V_{CC}=$V_{TH(MIN)}$ UM805/811LE/ME/JE			0.4	
		I_{SINK}=50μA, V_{CC}>1.0V			0.3	

Note 2: Production testing done at T_A=+25℃; limits over temperature guaranteed by design only.
Note 3: $\overline{RESET}$ output for UM805/811; RESET output for UM812.
Note 4: "Glitches" of 100ns or less typically will not generate a reset pulse.

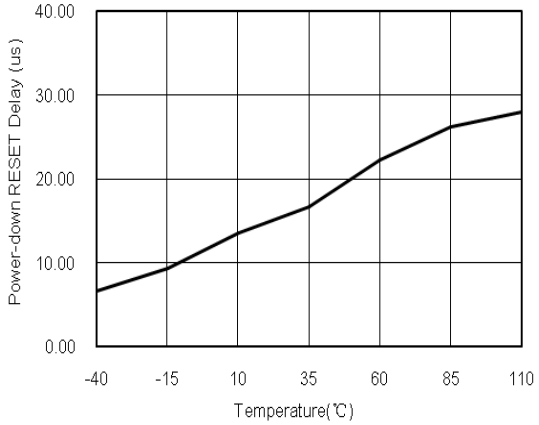
Typical Operating Characteristics

(T_A=+25℃, unless otherwise noted.)

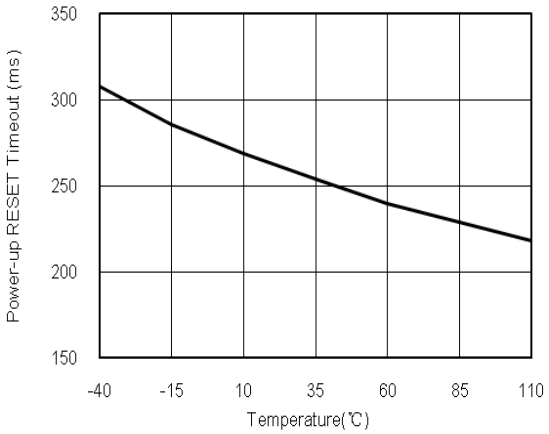
Supply Current vs. Temperature (UM811RE)



Power-down RESET Delay vs. Temperature (UM811RE)



Power-up RESET Timeout vs. Temperature



Detailed Description

RESET Timing

The reset signal is asserted LOW for the UM811 and HIGH for the UM812 when the power supply voltage falls below the threshold trip voltage and remains asserted for at least 140ms after the power supply voltage has risen above the threshold.

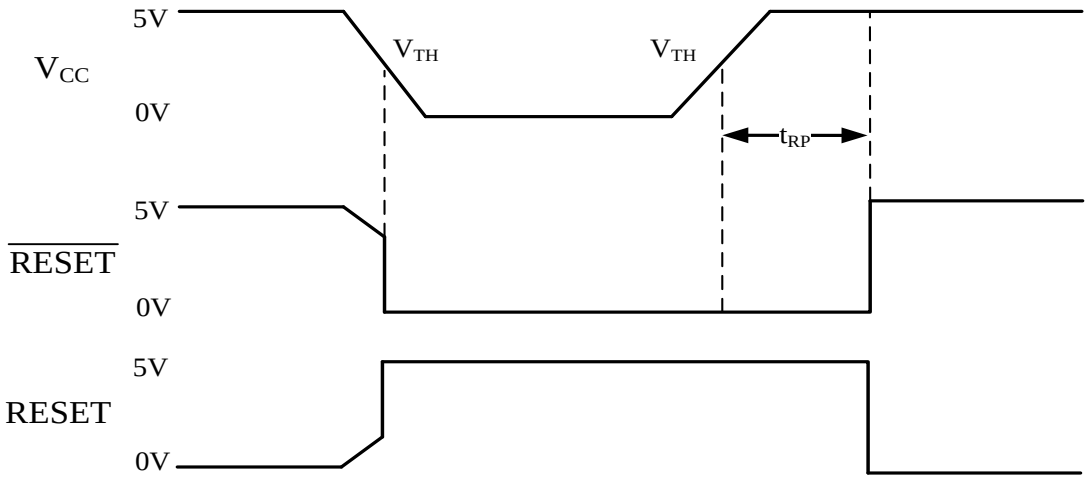


Figure 1. RESET vs. V_{CC} Timing Diagram

The reset signal is asserted LOW for the UM811 and HIGH for the UM812 when $\overline{MR}$ is low and remains asserted for at least 140ms after $\overline{MR}$ is high.

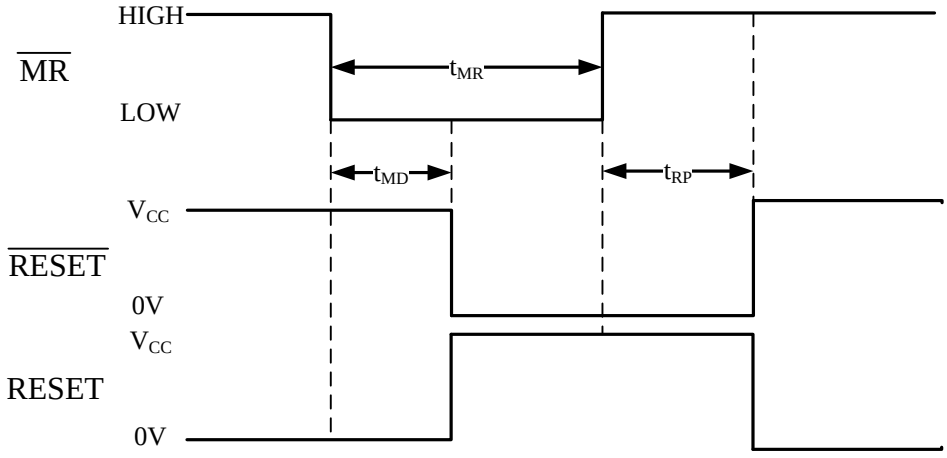


Figure 2. RESET vs. $\overline{MR}$ Timing Diagram

Reset Output

A microprocessor's (μP's) reset input starts the μP in a known state. These μP supervisory circuits assert reset to prevent code execution errors during power-up, power-down, or brownout conditions. $\overline{RESET}$ is guaranteed to be a logic low for V_{CC}>1V. Once V_{CC} exceeds the reset threshold, an internal timer keeps $\overline{RESET}$ low for the reset timeout period; after this interval, $\overline{RESET}$ goes high.
If a brownout condition occurs (V_{CC} dips below the reset threshold), $\overline{RESET}$ goes low. Any time

V_{CC} goes below the reset threshold, the internal timer resets to zero, and $\overline{RESET}$ goes low. The internal timer starts after V_{CC} returns above the reset threshold, and $\overline{RESET}$ remains low for the reset timeout period.
The manual reset input ($\overline{MR}$) can also initiate a reset. See the *Manual Reset Input* section.
The UM812 has an active-high RESET output that is the inverse of the UM805/811's $\overline{RESET}$ output. The UM805 uses an open-drain output, and the UM811/812 have a push-pull output stage. Connect a pull-up resistor on the UM805's $\overline{RESET}$ output to any supply between 0 and 6V.

Manual Reset Input

Many μP-based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{MR}$ asserts reset. Reset remains asserted while $\overline{MR}$ is low, and for the Reset Active Timeout Period (t_{RP}) after $\overline{MR}$ returns high. This input has an internal 20kΩ pull-up resistor, so it can be left open if it is not used. $\overline{MR}$ can be driven with TTL or CMOS-logic levels, or with open-drain/collector outputs. Connect a normally open momentary switch from $\overline{MR}$ to GND to create a manual-reset function; external debounce circuitry is not required. If $\overline{MR}$ is driven from long cables or if the device is used in a noisy environment, connecting a 0.1μF capacitor from $\overline{MR}$ to ground provides additional noise immunity.

Reset Threshold Accuracy

The UM805/811/812 are ideal for systems using a 5V±5% or 3V±5% power supply with ICs specified for 5V±10% or 3V±10%, respectively. They are designed to meet worst-case specifications over temperature. The reset is guaranteed to assert after the power supply falls out of regulation, but before power drops below the minimum specified operating voltage range for the system ICs. The thresholds are pre-trimmed and exhibit tight distribution, reducing the range over which an undesirable reset may occur.

Applications Information

Negative-Going V_{CC} Transients

In addition to issuing a reset to the µP during power-up, power-down, and brownout conditions, the UM805/811/812 are relatively immune to short-duration negative-going V_{CC} transients (glitches). Figure 3 shows typical transient duration vs. reset comparator overdrive, for which the UM805/811/812 do not generate a reset pulse. The graph was generated using a negative-going pulse applied to V_{CC}, starting above the actual reset threshold and ending below it by the magnitude indicated (reset comparator overdrive). The graph indicates the typical maximum pulse width a negative-going V_{CC} transient may have without causing a reset pulse to be issued. As the magnitude of the transient increases (goes farther below the reset threshold), the maximum allowable pulse width decreases. Typically, for the UM8_ _LE/ME/JE, a V_{CC} transient that goes 125mV below the reset threshold and lasts 40µs or less will not cause a reset pulse to be issued. A 0.1µF capacitor mounted as close as possible to the V_{CC} provides additional transient immunity.

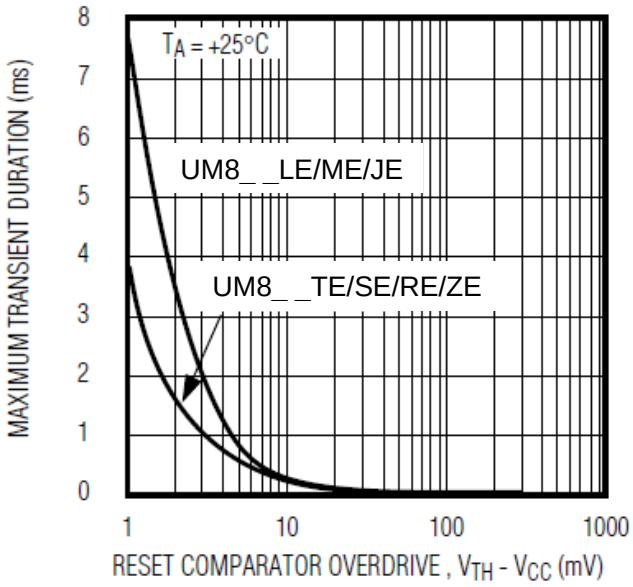


Figure 3. Maximum Transient Duration without Causing a Reset Pulse vs. Reset Comparator Overdrive

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to V_{CC}=0V

When V_{CC} falls below 1V, the UM811 $\overline{\text{RESET}}$ output no longer sinks current—it becomes an open circuit. Therefore, high-impedance CMOS-logic inputs connected to $\overline{\text{RESET}}$ can drift to undetermined voltages. This presents no problem in most applications since most µP and other circuitry is inoperative with V_{CC} below 1V. However, in applications where $\overline{\text{RESET}}$ must be valid down to 0V, adding a pull-down resistor to $\overline{\text{RESET}}$ pin will causes any stray leakage currents to flow to ground, holding $\overline{\text{RESET}}$ low (Figure 4). R1's value is not critical; 100kΩ is large enough not to load $\overline{\text{RESET}}$ and small enough to pull $\overline{\text{RESET}}$ to ground.
A 100kΩ pull-up resistor to V_{CC} is also recommended for the UM812 if RESET is required to remain valid for V_{CC}<1V.

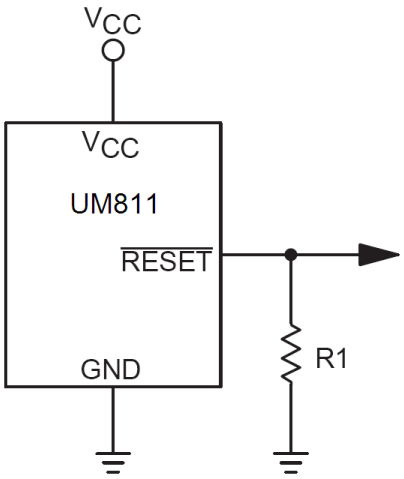


Figure 4. $\overline{\text{RESET}}$ Valid to V_{CC}=Ground Circuit

Interfacing to µPs with Bidirectional Reset Pins

µPs with bidirectional reset pins (such as the Motorola68HC11 series) can contend with the UM811/812 reset outputs. If, for example, the UM811 $\overline{\text{RESET}}$ output is asserted high and the µP wants to pull it low, indeterminate logic levels may result. To correct such cases, connect a 4.7kΩ resistor between the UM811 $\overline{\text{RESET}}$ (or UM812 RESET) output and the µP reset I/O (Figure 5). Buffer the reset output to other system components.

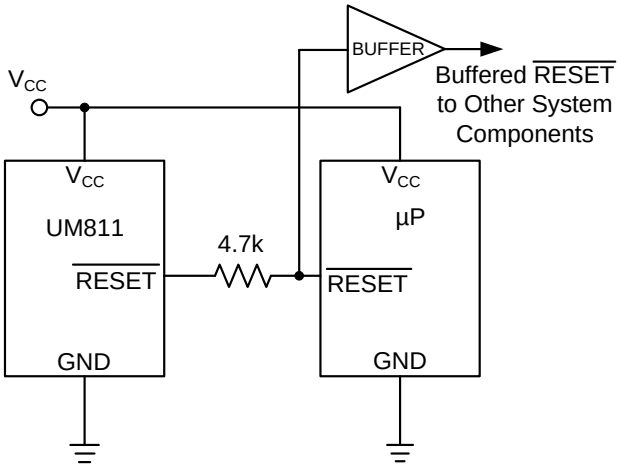


Figure 5. Interfacing to µPs with Bidirectional Reset I/O

UM805 Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Generally, the pull-up connected to the UM805 will connect to the supply voltage that is being monitored at the IC's V_{CC} pin. However, some systems may use the open-drain output to level-shift from the monitored supply to reset circuitry powered by some other supply (Figure 6). Note that as the UM805's V_{CC} decreases below 1V, so does the IC's ability to sink current at $\overline{\text{RESET}}$. Also, with any pull-up, $\overline{\text{RESET}}$ will be pulled high as V_{CC} decays toward 0. The voltage where this occurs depends on the pull-up resistor value and the voltage to which it is connected.

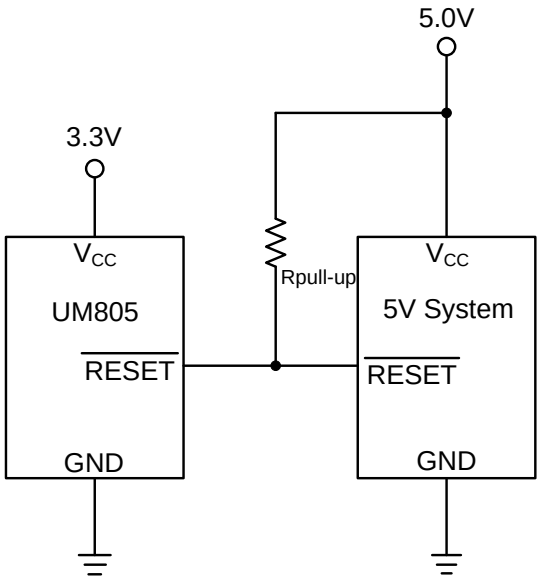
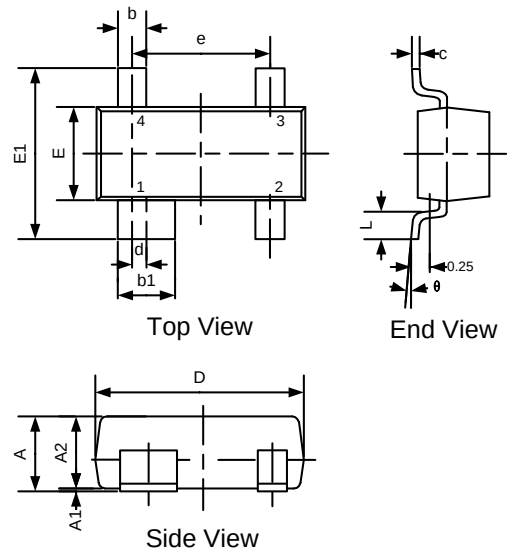


Figure 6. UM805 Open-Drain $\overline{\text{RESET}}$ Output Allows Use with Multiple Supplies

Package Information

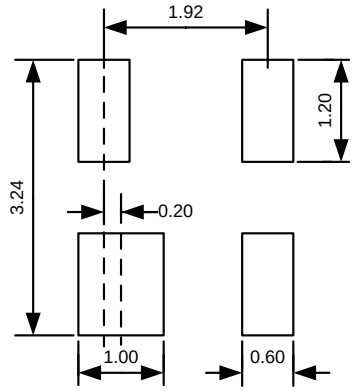
SOT143

Outline Drawing



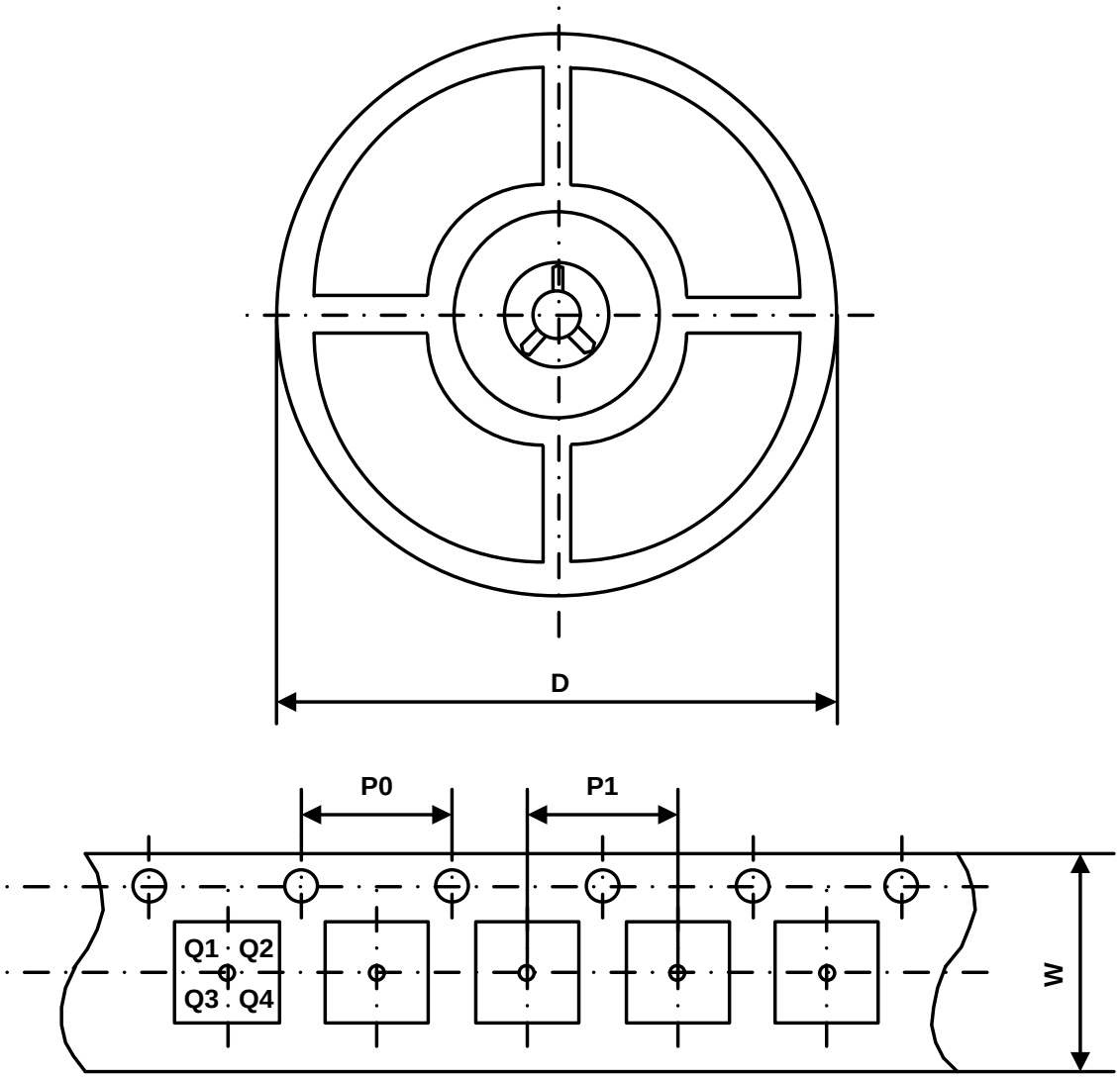
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.80	-	1.22	0.031	-	0.048
A1	0.00	-	0.15	0.000	-	0.006
A2	0.75	-	1.07	0.030	-	0.042
b	0.30	0.40	0.51	0.012	0.016	0.020
b1	0.75	-	0.93	0.030	-	0.037
c	0.08	-	0.20	0.003	-	0.008
d	0.20TYP			0.008TYP		
D	2.80	2.90	3.04	0.110	0.114	0.120
E	1.20	1.30	1.40	0.047	0.051	0.055
E1	2.20	-	2.64	0.087	-	0.104
e	1.92BSC			0.076BSC		
L	0.30	-	0.60	0.012	-	0.024
θ	0 º	-	8 º	0 º	-	8 º

Land Pattern



NOTES:
1. Compound dimension: 2.90×1.30;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM805xx	SOT143	8 mm	4 mm	2 mm	180 mm	Q1
UM811xx	SOT143	8 mm	4 mm	4 mm	180 mm	Q3
UM812xx	SOT143	8 mm	4 mm	4 mm	180 mm	Q3

Selection Table

Part Number	RESET Threshold (V)	Timeout Period (ms)	Output Type	Marking Code	Package Type	Shipping Qty
UM805LE	4.63	240	Open-Drain, Active Low	05L	SOT143	3000pcs/7Inch Tape & Reel
UM805ME	4.38	240	Open-Drain, Active Low	05M		
UM805JE	4.00	240	Open-Drain, Active Low	05J		
UM805TE	3.08	240	Open-Drain, Active Low	05T		
UM805SE	2.93	240	Open-Drain, Active Low	05S		
UM805RE	2.63	240	Open-Drain, Active Low	05R		
UM805ZE	2.32	240	Open-Drain, Active Low	05Z		
UM811LE	4.63	240	Push-Pull, Active Low	11L		
UM811ME	4.38	240	Push-Pull, Active Low	11M		
UM811JE	4.00	240	Push-Pull, Active Low	11J		
UM811TE	3.08	240	Push-Pull, Active Low	11T		
UM811SE	2.93	240	Push-Pull, Active Low	11S		
UM811RE	2.63	240	Push-Pull, Active Low	11R		
UM811ZE	2.32	240	Push-Pull, Active Low	11Z		
UM812LE	4.63	240	Push-Pull, Active High	12L		
UM812ME	4.38	240	Push-Pull, Active High	12M		
UM812JE	4.00	240	Push-Pull, Active High	12J		
UM812TE	3.08	240	Push-Pull, Active High	12T		
UM812SE	2.93	240	Push-Pull, Active High	12S		
UM812RE	2.63	240	Push-Pull, Active High	12R		
UM812ZE	2.32	240	Push-Pull, Active High	12Z		

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