

单通道、低电容双向TVS 保护二极管

UM5084 DFN2 1.0×0.6

描述

UM5084 TVS 保护二极管设计用于取代手机、笔记本电脑和 PDA 等便携式应用中 MLV。与 MLV 相比，该器件内置可传导高瞬态电流的大截面积结，具有板级保护的电气特性，包括快速响应时间、较低的工作电压、较低的钳位电压和无器件劣化。

UM5084 TVS 保护二极管可保护敏感半导体元件免受静电放电 (ESD) 和其他瞬态电压事件造成的损坏或破坏。UM5084 采用 DFN2 1.0×0.6 (与 SOD923/SOD882/CSP 1.0×0.6 兼容) 封装，工作电压为 12 V。在阵列不实用的应用中，设计人员可灵活地使用该器件保护一条双向单线。此外，在电路板空间有限的应用中，该器件可采用分散布置的布局方案。UM5084 可满足 IEC 61000-4-2 标准的静电抗扰度要求：±15kV 空气间隙放电和 ±8kV 接触放电。

应用

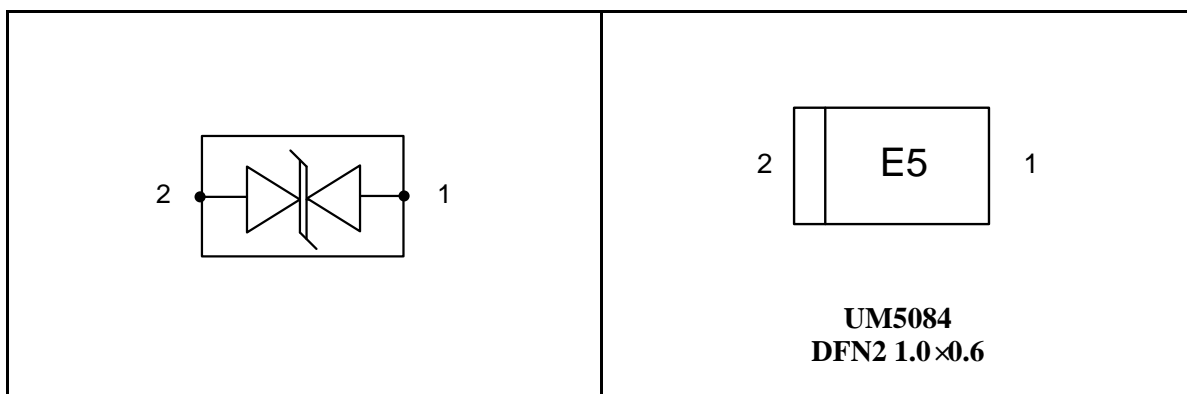
- 手机听筒和配件
- PDA
- 笔记本电脑、台式机和服务
- 便携式设备
- 无线电话
- 智能卡
- 数码相机
- MP3 播放器

特性

- 数据线瞬态保护，符合IEC 61000-4-2标准：±15kV（空气间隙放电），±8kV（接触放电）
- 用于便携式电子设备的小型封装
- ESD保护应用中MLV的合适替代品
- 双向TVS保护
- 反向工作电压：12V
- 低漏电流
- 低二极管电容
- 小外形尺寸：1.0mm×0.6mm

引脚配置

顶部视图



Ordering Information

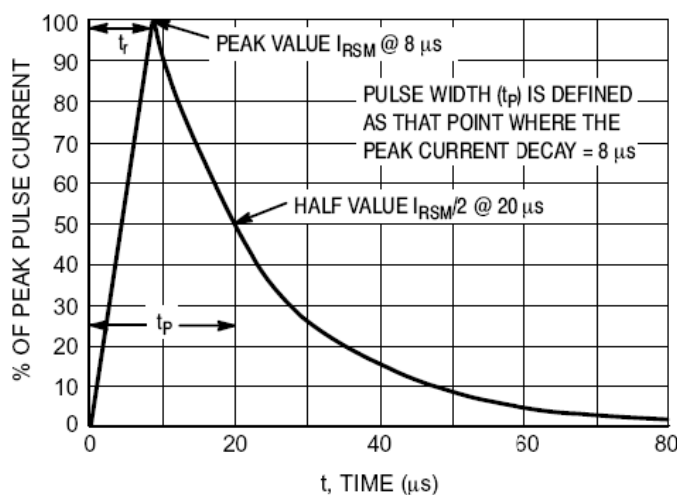
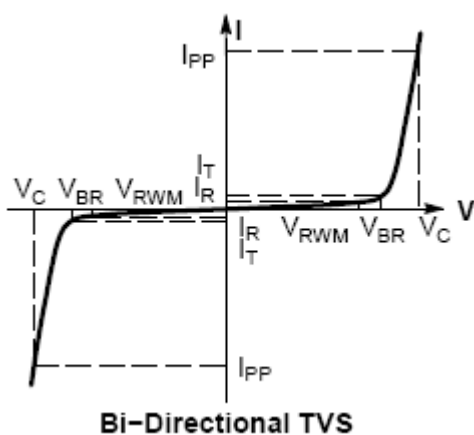
Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5084	12.0V	DFN2 1.0×0.6	1	E5	5000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Peak Pulse Power ($t_p=8/20\mu s$)	P_{PK}	140	Watts
Maximum Peak Pulse Current ($t_p=8/20\mu s$)	I_{PP}	5.9	Amps
Lead Soldering Temperature	T_L	260 (10 sec.)	°C
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Symbol Definition

Parameter	Symbol
Maximum Reverse Peak Pulse Current	I_{PP}
Clamping Voltage @ I_{PP}	V_C
Working Peak Reverse Voltage	V_{RWM}
Maximum Reverse Leakage Current @ V_{RWM}	I_R
Breakdown Voltage @ I_T	V_{BR}
Test Current	I_T
Peak Power Dissipation	P_{PK}
Max. Capacitance @ $V_R=0V$, $f=1MHz$	C_J



Electrical Characteristics

(T=25 °C, Device for 12.0V Reverse Stand-off Voltage)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}				12	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$	16.7		18.7	V
Reverse Leakage Current	I_R	$V_{RWM}=12V$, $T=25\text{ }^{\circ}C$			0.5	μA
Clamping Voltage	V_C	$I_{PP}=5.9A$, $t_P=8/20\mu s$			23.7	V
Junction Capacitance	C_J	$V_R=0V$, $f=1MHz$		10	15	pF

Applications Information**Device Connection Options**

UM5084 ESD protection diode is designed to protect one bidirectional data, I/O or power supply line from the damage caused by ESD and surge pulses. The device is bidirectional and may be used on lines where the signal polarity is above ground and below ground.

Circuit Board Layout Recommendations for Suppression of ESD

Good circuit board layout is critical for the suppression of ESD induced transients. The following guidelines are recommended:

1. Place the TVS near the input terminals or connectors to restrict transient coupling.
2. Minimize the path length between the TVS and the protected line.
3. Minimize all conductive loops including power and ground loops.
4. The ESD transient return path to ground should be kept as short as possible.
5. Never run critical signals near board edges.
6. Use ground planes whenever possible. For multilayer printed-circuit boards, use ground vias.
7. Keep parallel signal paths to a minimum.
8. Avoid running protection conductors in parallel with unprotected conductor.
9. Avoid using shared transient return paths to a common ground point.

Package Information

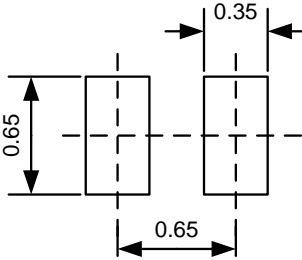
UM5084 DFN2 1.0×0.6

Outline Drawing

DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.40	-	0.53	0.016	-	0.021
A1	0.00	-	0.05	0.000	-	0.002
b	0.45	0.50	0.55	0.018	0.020	0.022
D	0.95	1.00	1.075	0.037	0.039	0.042
E	0.55	0.60	0.675	0.022	0.024	0.027
e	0.65TYP			0.026TYP		
L	0.20	0.25	0.30	0.008	0.010	0.012
L1	0.00	0.05	0.10	0.000	0.002	0.004
R	0.05	0.10	0.15	0.002	0.004	0.006

Note: R is optional.

Land Pattern

	<p>NOTES:</p> <ol style="list-style-type: none"> Compound dimension: 1.00×0.60 ; Unit: mm; General tolerance $\pm 0.05\text{mm}$ unless otherwise specified; The layout is just for reference.
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Tape and Reel Orientation



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