3.3 V Differential Multipoint Low Voltage M-LVDS Driver Receiver

UM3405 ***SOP8***
UM3406 ***SOP8***

1 Description

UM3405 and UM3406 are pure 3.3V supply differential Multipoint Low Voltage (M-LVDS) line Drivers and Receivers. UM3405 and UM3406 are TIA/EIA-899 compliant. The UM3405 offers Type 1 receiver threshold at 0.0V. The UM3406 offers Type 2 receiver threshold at 0.1 V.

The devices have Type 1 and Type 2 receivers that detect the bus state with as little as 50 mV of differential input voltage over a common-mode voltage range of -1V to 3.4V. The Type 1 receivers have near zero thresholds (±50 mV) and exhibit 25 mV of differential input voltage hysteresis to prevent output oscillations with slowly changing signals or loss of input. The Type 2 receivers include an offset threshold to provide a detectable voltage under open-circuit, idle-bus, and other faults conditions. UM3405 and UM3406 support Simplex or Half Duplex bus configurations.

2 Applications

- Low-Power High-Speed Short-Reach Alternative to TIA/EIA-485
- Backplane or Cabled Multipoint Data and Clock Transmission
- Cellular Base Stations
- Central-Office Switches
- Network Switches and Routers

3 Features

- Low-Voltage Differential 30 Ω to 55 Ω Line Drivers and Receivers for Signaling Rates Up to 200 Mbps
- Type 1 Receivers Incorporate 25 mV of Hysteresis
- Type 2 Receivers Provide an Offset (100 mV) Threshold to Detect Open-Circuit and Idle-Bus Conditions
- Meets or Exceeds the M-LVDS Standard TIA/EIA-899 for Multipoint Data Interchange
- Controlled Driver Output Voltage Transition Times for Improved Signal Quality
- -1 V to 3.4 V Common-Mode Voltage Range Allows Data Transfer with up to 2 V of Ground Noise
- Bus Pins High Impedance When Disabled or $V_{CC} \leq 1.5$ V
- M-LVDS Bus Power Up/Down Glitch Free
- Operating range: V_{CC} = 3.3 ±10% V (3.0 to 3.6V)
- Operating temperature range: -40℃ to 125℃
- Latch-up performance exceeds 200 mA per JESD 78

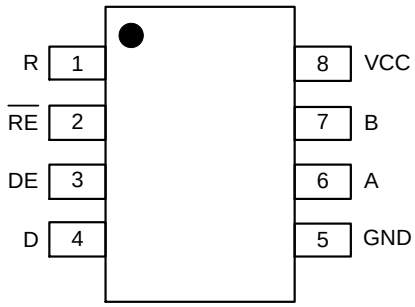
4 Selection Guide

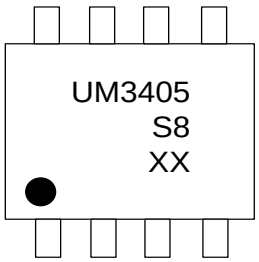
Part Number	Receiver Type	Max Data Rate (Mbps)	V_{CC} Range (V)
UM3405S8	Type 1	200	3.0 to 3.6
UM3406S8	Type 2	200	3.0 to 3.6

5 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UM3405S8	UM3405S8	SOP8	3000pcs/13Inch Tape & Reel
UM3406S8	UM3406S8	SOP8	3000pcs/13Inch Tape & Reel

6 Pin Configuration and Function





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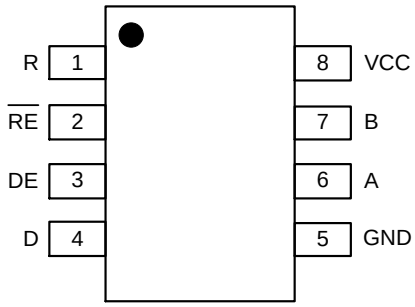
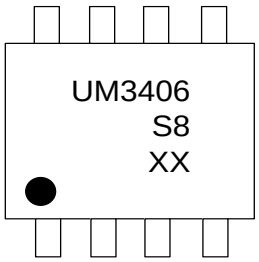




XX: Week Code
UM3406S8
SOP8

6 Pin Configuration and Function (continued)

Pin No.	Pin Name	I/O Type	Open Default	Function
1	R	LVCMOS Output		Receiver Output Pin
2	$\overline{RE}$	LVCMOS Input	HIGH	Receiver Enable Input Pin (Low=Active, High=High Z Output)
3	DE	LVCMOS Input	LOW	Driver Enable Input Pin (Low=High Z Output, High=Active)
4	D	LVCMOS Input		Driver Input Pin
5	GND			Ground Supply pin. Pin must be connected to power supply to guarantee proper operation.
6	A	M-LVDS Input/Output		Transceiver True Input/Output Pin
7	B	M-LVDS Input/Output		Transceiver Invert Input/Output Pin
8	VCC			Power Supply pin. Pin must be connected to power supply to guarantee proper operation.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply voltage		-0.5		4.0	V
V_{IN}	Input Voltage on any logic pin (D, DE , $\overline{RE}$)		-0.3		4.0	V
	Input Voltage on A, B		-1.8		4.0	V
V_{OUT}	Output Voltage R		-0.3		V_{CC}+0.3	V
	Output Voltage A, B		-1.8		4.0	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002	All pins		±2		kV
T_{STG}	Storage temperature		-65		150	℃

Note 1: Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
Note 2: Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and not valid simultaneously. If stress limits are exceeded device functional operation is not implied, damage may occur and reliability may be affected.

7.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{BUS}	Voltage at any bus terminal V_A, V_B		-1.4		3.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.05		V_{CC}	V
T_A	Operating free-air temperature		-40		125	℃

7.3 Thermal Characteristics

Symbol	Thermal Metric	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	110	℃/W
θ_{JC}	Junction-to-case thermal resistance	54	

7.4 Electrical Characteristics (Static) (Note 1)

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	Power Supply Current	Receiver Disabled and Driver Enabled. $\overline{RE}$ and DE = V_{CC}; R_L = 50 Ω; All others open		13	22	mA
		Receiver and Driver Disabled. $\overline{RE}$ = V_{CC}; DE = GND; R_L = No load; All others open		1	4	
		Receiver and Driver Enabled. $\overline{RE}$ = GND; DE = V_{CC}; R_L = 50 Ω; All others open		16	24	
		Receiver Enabled and Driver Disabled. $\overline{RE}$ and DE = V_{CC}; R_L = 50 Ω; All others open			13	

7.4 Electrical Characteristics (Static) (Note 1) (continued)

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Level		2		V_{CC}	V
V_{IL}	Input Low Level		GND		0.8	V
V_{BUS}	Voltage at any bus terminal V_A, V_B		-1.4		3.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage		0.05		V_{CC}	V
Driver						
$\|V_{AB}\|$	Differential output voltage magnitude	see Figure 8-2	480		650	mV
$\Delta\|V_{AB}\|$	Change in Differential output voltage magnitude between logic states	see Figure 8-2	-50		50	mV
$V_{OS(SS)}$	Steady state common mode output voltage	see Figure 8-3	0.8		1.2	V
$\Delta V_{OS(SS)}$	Change in Steady state common mode output voltage between logic states	see Figure 8-3	-50		50	mV
$V_{OS(PP)}$	Peak-to-peak common-mode output voltage	see Figure 8-3			150	mV
V_{AOC}	Maximum steady-state open-circuit output voltage	see Figure 8-7	0		2.4	V
V_{BOC}	Maximum steady-state open-circuit output voltage	see Figure 8-7	0		2.4	V
$V_{P(H)}$	Voltage overshoot, low-to-high level output	see Figure 8-5			$1.2V_{SS}$	V
$V_{P(L)}$	Voltage overshoot, high-to-low level output	see Figure 8-5	$-0.2V_{SS}$			V
I_{IH}	High-level input current (D, DE)	V_{IH} = 2V	0		10	μA
I_{IL}	Low-level input current (D, DE)	V_{IL} = 0.8V	0		10	μA
$\|I_{OS}\|$	Differential short−circuit output current magnitude	see Figure 8-4			24	mA
Receiver						
V_{IT+}	Positive-going Differential Input voltage Threshold (See Figure 8-9 and Tables 9-1 and 9-2)	Type 1			50	mV
		Type 2			150	
V_{IT-}	Negative-going Differential Input voltage Threshold (See Figure 8-9 and Tables 9-1 and 9-2)	Type 1	-50			mV
		Type 2	50			

7.4 Electrical Characteristics (Static) (Note 1) (continued)

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
V_{HYS}	Differential Input Voltage Hysteresis (See Figure 8-9)	Type 1		25		mV
		Type 2		0		
V_{OH}	High-level output voltage	I_{OH} = -8 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			0.4	V
I_{IH}	High-level input current ($\overline{RE}$)	V_{IH} = 2V	-10		0	μA
I_{IL}	Low-level input current ($\overline{RE}$)	V_{IL} = 0.8V	-10		0	μA
I_{OZ}	High-impedance state output current	V_O = 0V or VCC	-10		15	μA
C_A/C_B	Input Capacitance	V_I = 0.4 sin(30E^{6}πt) + 0.5 V, other outputs at 1.2V (Note 2)		3		pF
C_{AB}	Differential Input Capacitance	V_{AB} = 0.4 sin(30E^{6}πt) V, other outputs at 1.2V (Note 2)			2.5	pF
$C_{A/B}$	Input Capacitance Balance, (C_A/C_B)		99		101	%
Bus Input and Output						
I_A	Input Current Receiver or Transceiver with Driver Disabled	V_A= 3.8V, V_B= 1.2V	0		32	μA
		V_A= 0V or 2.4V, V_B= 1.2V	-20		20	
		V_A= -1.4V, V_B= 1.2V	-32		0	
I_B	Input Current Receiver or Transceiver with Driver Disabled	V_B= 3.8V, V_A= 1.2V	0		32	μA
		V_B= 0V or 2.4V, V_A= 1.2V	-20		20	
		V_B= -1.4V, V_A= 1.2V	-32		0	
I_{AB}	Differential Input Current Receiver or Transceiver with driver disabled (I_A-I_B)	$V_A = V_B$, $-1.4 \le V_A \le 3.8$ V	-4		4	μA

7.4 Electrical Characteristics (Static) (Note 1) (continued)

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Bus Input and Output						
$I_{A(OFF)}$	Input Current Receiver or Transceiver Power Off	$0V \le V_{CC} \le 1.5$, V_A= 3.8V, V_B= 1.2V	0		32	μA
		$0V \le V_{CC} \le 1.5$, V_A= 0V or 2.4V, V_B= 1.2V	-20		20	
		$0V \le V_{CC} \le 1.5$, V_A= -1.4V, V_B= 1.2V	-32		0	
$I_{B(OFF)}$	Input Current Receiver or Transceiver Power Off	$0V \le V_{CC} \le 1.5$, V_B= 3.8V, V_A= 1.2V	0		32	μA
		$0V \le V_{CC} \le 1.5$, V_B= 0V or 2.4V, V_A= 1.2V	-20		20	
		$0V \le V_{CC} \le 1.5$, V_B= -1.4V, V_A= 1.2V	-32		0	
$I_{AB(OFF)}$	Receiver Input or Transceiver Input/Output Power Off Differential Input Current (I_A-I_B)	$0V \le V_{CC} \le 1.5$, $V_A = V_B$, $-1.4 \le V_A \le 3.8$ V	-4		4	μA
C_A	Transceiver Input Capacitance with Driver Disabled	V_A = 0.4 sin(30E^{6}πt) + 0.5 V (Note 2); V_B = 1.2 V		5		pF
C_B	Transceiver Input Capacitance with Driver Disabled	V_B = 0.4 sin(30E^{6}πt) + 0.5 V (Note 2); V_A = 1.2 V		5		pF
C_{AB}	Transceiver Input Capacitance with Driver Disabled	V_A = 0.4 sin(30E^{6}πt) +0.5 V (Note 2); V_B = 1.2 V			3	pF
$C_{A/B}$	Transceiver Input Capacitance Balance with Driver Disabled, (C_A/C_B)		99		101	%

Note 1: The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
Note 2: HP4194A impedance analyzer (or equivalent)

7.5 Electrical Characteristics (Dynamic)

7.5.1 Electrical Characteristics (Dynamic)—Driver

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8-5	1	1.9	2.6	ns
t_{PHL}	Propagation delay time, high-to-low-level output		1	1.9	2.6	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 8-6			7	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output				7	ns
t_{PZH}	Enable time, high-impedance-to-high-level output				7	ns
t_{PZL}	Enable time, high-impedance-to-low-level output				7	ns
$t_{SK(P)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	See Figure 8-5		0	120	ps
$t_{SK(PP)}$	Part-to-part skew (Note 1)	See Figure 8-5			1	ns
$t_{JIT(PER)}$	Period jitter rms (Note 2)	100 MHz clock input (Note 3), see Figure 8-8		2	3	ps
$t_{JIT(PP)}$	Peak-to-peak jitter (Note 2)	200 Mbps 2^{15}-1 PRBS input (Note 4), see Figure 8-8		30	130	ps
t_R	Differential output signal rise time	See Figure 8-5	1		1.6	ns
t_F	Differential output signal fall time	See Figure 8-5	1		1.6	ns

Note 1: $t_{SK(PP)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
Note 2: Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
Note 3: $t_R = t_F$ =0.5 ns (10% and 90%). Source jitter de-embedded from Output values.

7.5.2 Electrical Characteristics (Dynamic)—Receiver

V_{CC} = 3.3V ±10% (3V to 3.6V), GND = 0V, T_A = -40°C to +125°C. All typical values are at 25°C and supply voltage of V_{CC}= 3.3 V.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Receiver							
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 8-10		2	5.2	6.8	ns
t_{PHL}	Propagation delay time, high-to-low-level output			2	5.2	6.8	ns
t_{PHZ}	Disable time, high-level-to-high-impedance output	See Figure 8-11				10	ns
t_{PLZ}	Disable time, low-level-to-high-impedance output					10	ns
t_{PZH}	Enable time, high-impedance-to-high-level output					15	ns
t_{PZL}	Enable time, high-impedance-to-low-level output					15	ns
$t_{SK(P)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	C_L=15pF, See Figure 8-10	Type1		100	300	ps
			Type2		300	500	
$t_{SK(PP)}$	Part-to-part skew (Note 1)	C_L=15pF, see Figure 8-10				1	ns
$t_{JIT(PER)}$	Period jitter rms (Note 2)	100 MHz clock input (Note 3), see Figure 8-12			4	7	ps
$t_{JIT(PP)}$	Peak-to-peak jitter (Note 2)	200 Mbps 2^{15}-1 PRBS input (Note 4), see Figure 8-12	Type1		200	700	ps
			Type2		225	800	
t_R	Differential output signal rise time	C_L=15pF, see Figure 8-10		1		2.6	ns
t_F	Differential output signal fall time	C_L=15pF, see Figure 8-10		1		2.6	ns

Note 1: $t_{SK(PP)}$ is the magnitude of the time difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
Note 2: Jitter is ensured by design and characterization. Stimulus jitter has been subtracted from the numbers.
Note 3: V_{ID} = 200 mV_{PP}, V_{CM} =1 V, t_R= t_F =0.5 ns (10% and 90%). Source jitter de-embedded from Output values
Note 4: t_R = t_F =0.5 ns (10% and 90%). Source jitter de-embedded from Output values.

8 Parameter Measurement Information

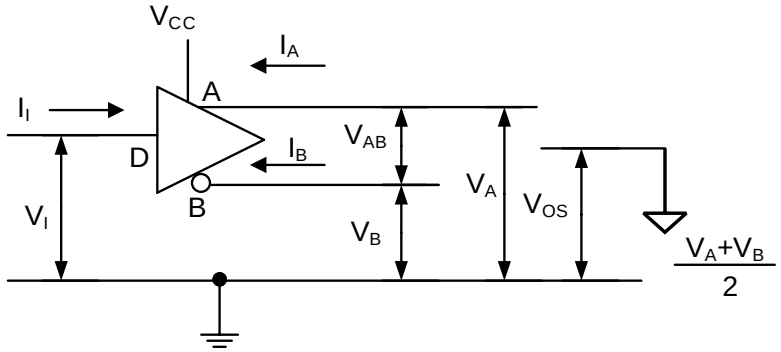
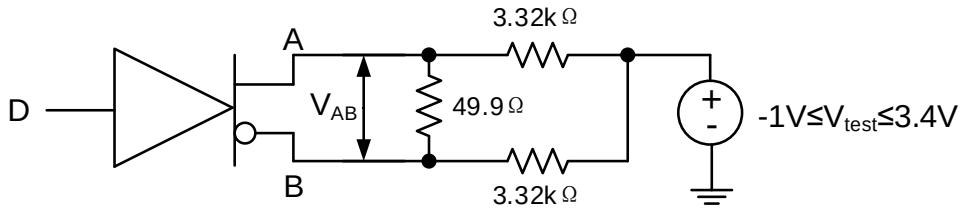
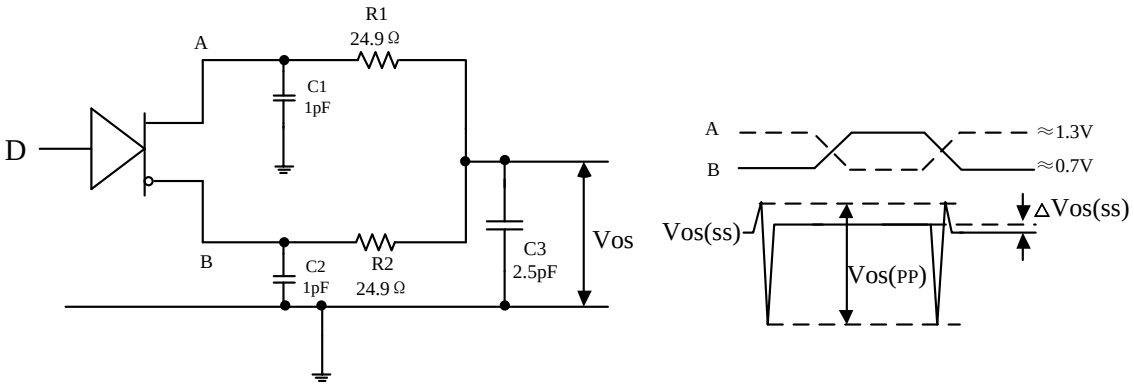


Figure 8-1. Driver Voltage and Current Definitions



Note: All resistors are 1% tolerance.

Figure 8-2. Differential Output Voltage Test Circuit



Note 1: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \leq$ 1ns, frequency = 500 kHz, duty cycle = 50±5%.
Note 2: C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20% tolerance.
Note 3: R1 and R2 are metal film, surface mount, 1% tolerance, and located within 2 cm of the D.U.T.
Note 4: The measurement of $V_{OS(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 8-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

8 Parameter Measurement Information (continued)

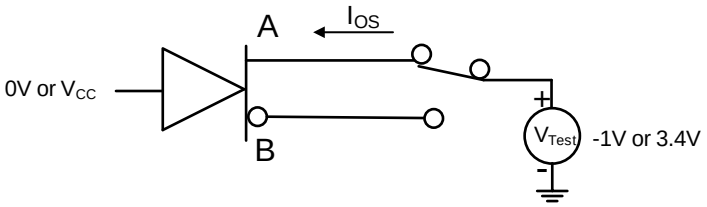
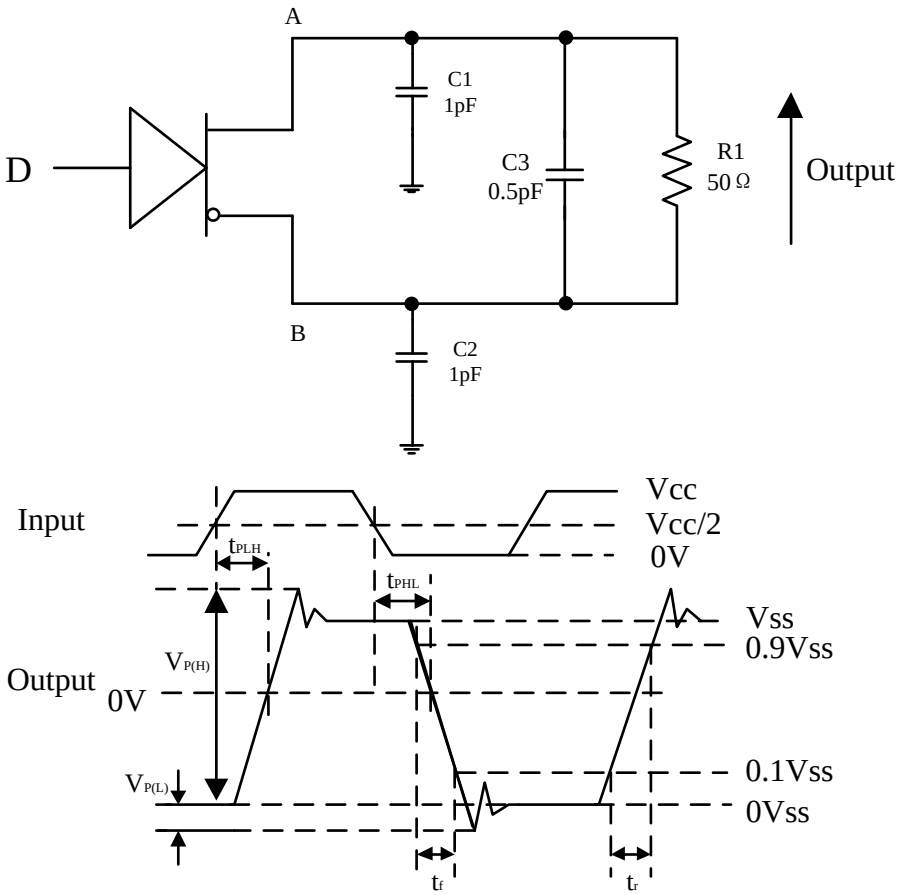


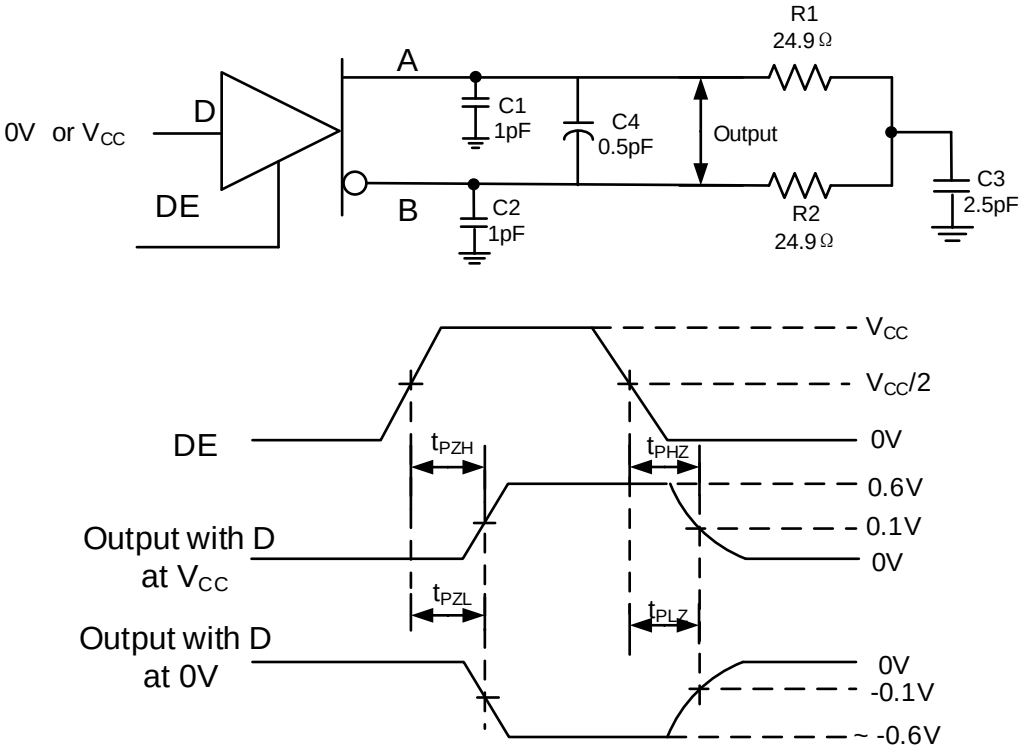
Figure 8-4. Driver Short-Circuit Test Circuit



Note 1: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \leq$ 1ns, frequency = 500 kHz, duty cycle = 50±5%.
Note 2: C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
Note 3: R1 is a metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
Note 4: The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 8-5. Driver Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal

8 Parameter Measurement Information (continued)



Note 1: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \leq$ 1ns, frequency = 500 kHz, duty cycle = 50±5%.
Note 2: C1, C2 and C3 include instrumentation and fixture capacitance within 2 cm of the D.U.T. and are 20%.
Note 3: R1 and R2 are metal film, surface mount, and 1% tolerance and located within 2 cm of the D.U.T.
Note 4: The measurement is made on test equipment with a -3 dB bandwidth of at least 1 GHz.

Figure 8-6. Driver Enable and Disable Time Circuit and Definitions

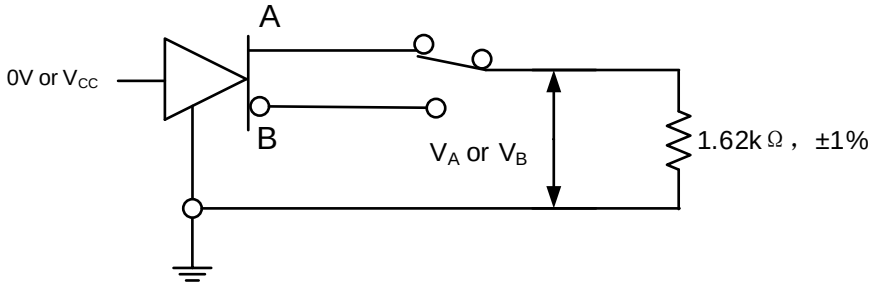
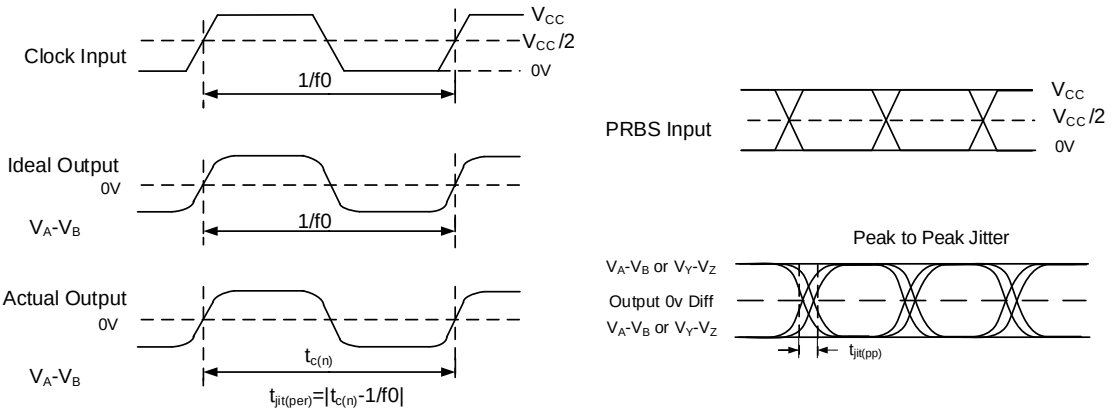


Figure 8-7. Maximum Steady State Output Voltage

8 Parameter Measurement Information (continued)



Note 1: All input pulses are supplied by an Agilent 8304A Stimulus System.
Note 2: The measurement is made on a TEK TDS6604 running TDSJIT3 application software
Note 3: Period jitter is measured using a 100 MHz 50 ±1% duty cycle clock input.
Note 4: Peak-to-peak jitter is measured using a 200 Mbps 2^{15}–1 PRBS input.

Figure 8-8. Driver Jitter Measurement Waveforms

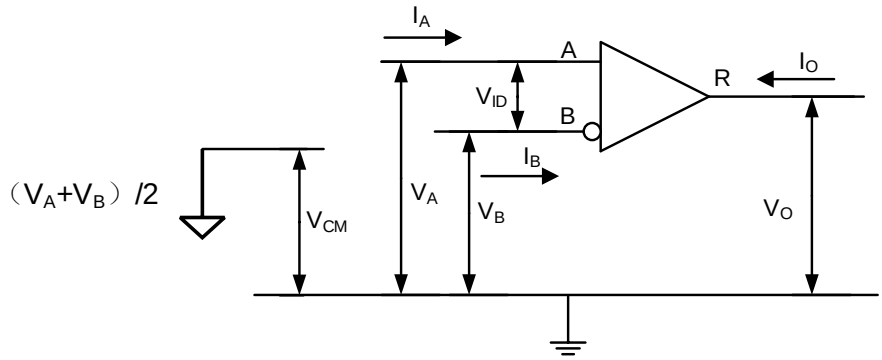
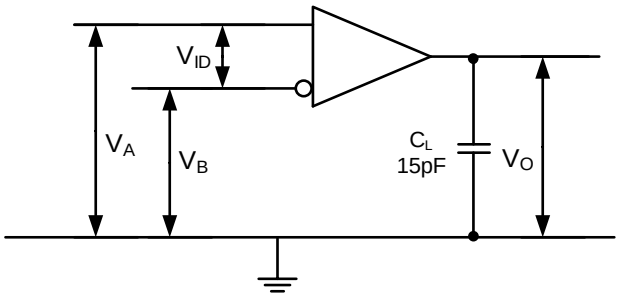
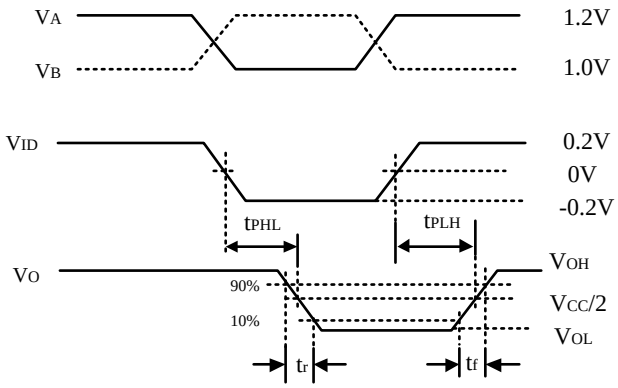


Figure 8-9. Receiver Voltage and Current Definitions

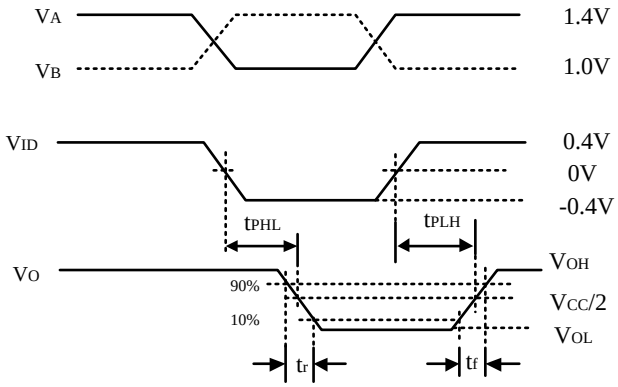
8 Parameter Measurement Information (continued)



Type 1



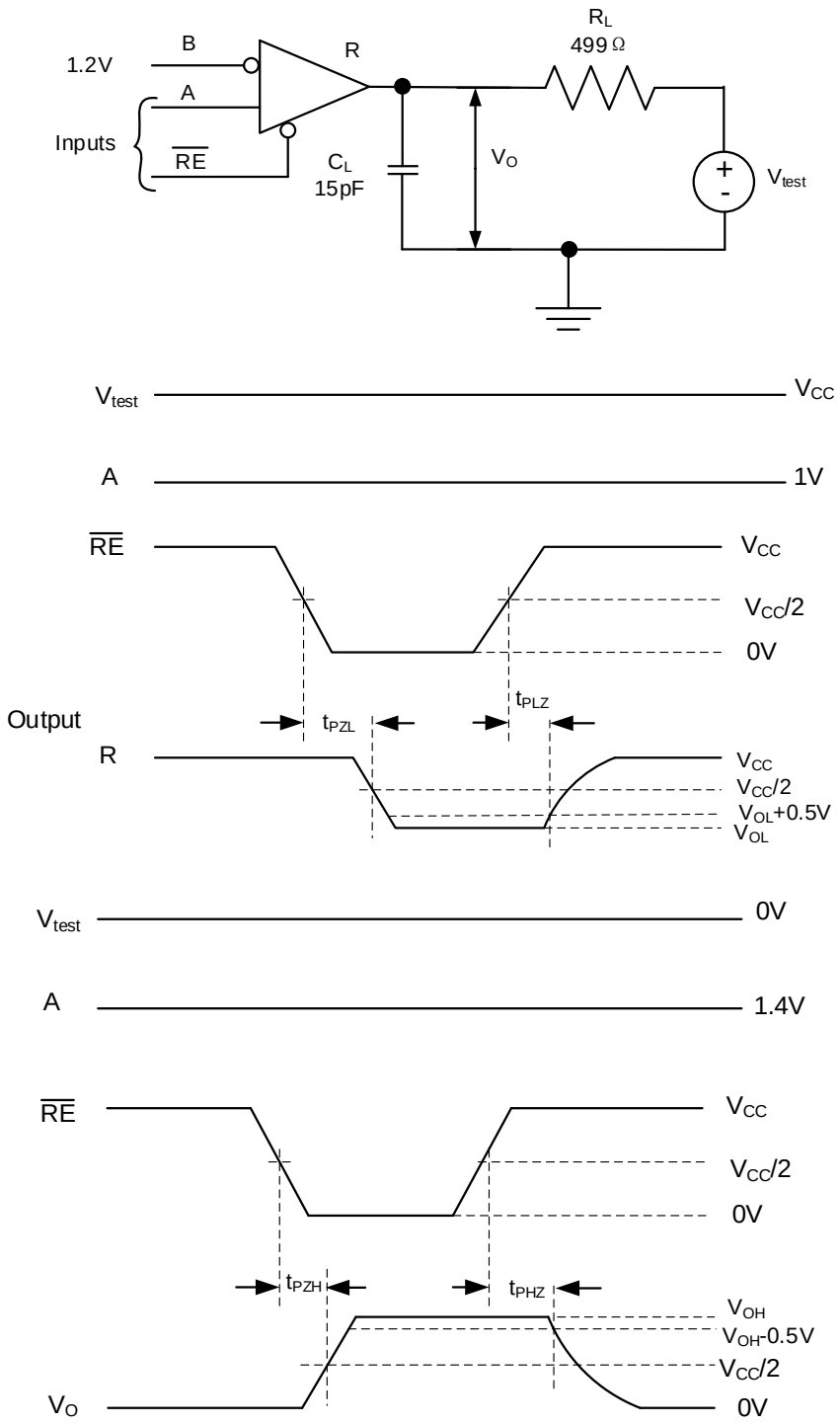
Type 2



Note 1: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \leq$ 1 ns, frequency = 1 MHz, duty cycle = 50±5%. C_L is a combination of a 20% tolerance, low-loss ceramic, surface-mount capacitor and fixture capacitance within 2 cm of the D.U.T.
Note 2: The measurement is made on test equipment with a –3 dB bandwidth of at least 1 GHz.

Figure 8-10. Receiver Timing Test Circuit and Waveforms

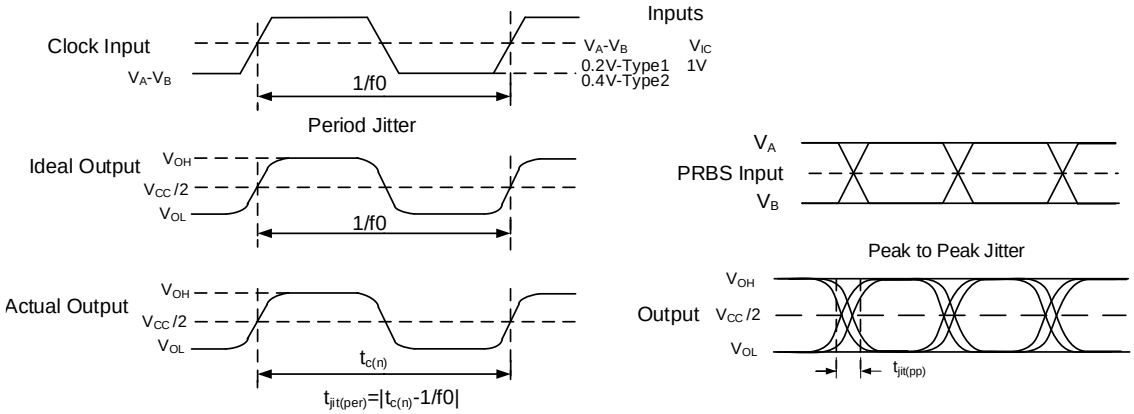
8 Parameter Measurement Information (continued)



Note 1: All input pulses are supplied by a generator having the following characteristics: t_R or $t_F \leq$ 1 ns, frequency = 500 kHz, duty cycle = 50 ±5%.
Note 2: R_L is 1% tolerance, metal film, surface mount, and located within 2 cm of the D.U.T.
Note 3: C_L is the instrumentation and fixture capacitance within 2 cm of the DUT and 20%.

Figure 8-11. Receiver Enable/Disable Time Test Circuit and Waveforms

8 Parameter Measurement Information (continued)



Note 1: All input pulses are supplied by an Agilent 8304A Stimulus System.
Note 2: The measurement is made on a TEK TDS6604 running TDSJIT3 application software
Note 3: Period jitter is measured using a 100 MHz 50±1% duty cycle clock input.
Note 4: Peak-to-peak jitter is measured using a 200 Mbps $2^{15}-1$ PRBS input.

Figure 8-12. Receiver Jitter Measurement Waveforms

8 Parameter Measurement Information (continued)

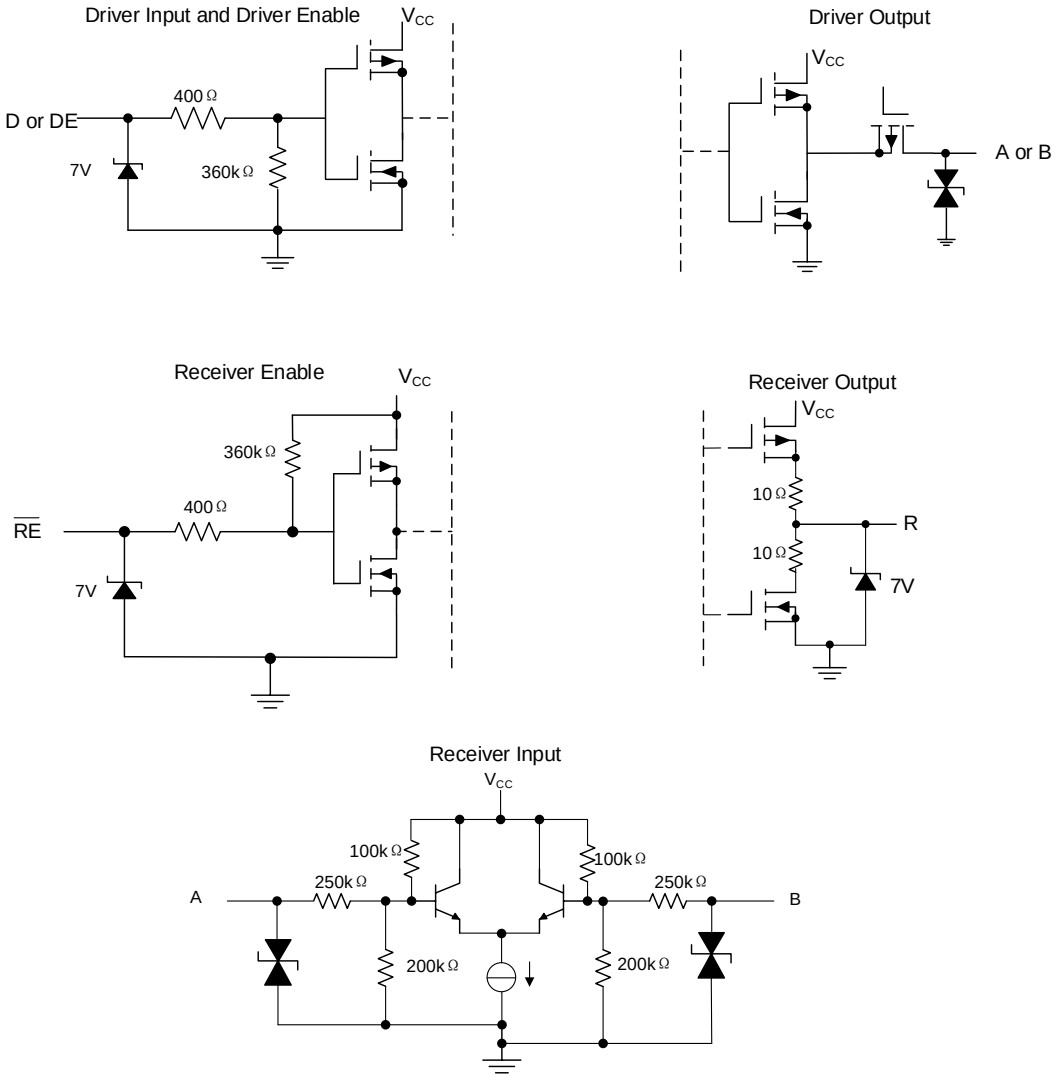


Figure 8-13. Equivalent Input and Output Schematic Diagrams

9 Detailed Description

9.1 Receiver Input Threshold Test Voltages

Table 9-1. Type 1 Receiver Input Threshold Test Voltages

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output (Note 1)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.800	3.750	0.050	3.775	H
3.750	3.800	-0.050	3.775	L
-1.350	-1.400	0.050	-1.375	H
-1.400	-1.350	-0.050	-1.375	L

Note 1: H = High level, L = Low level, output state assumes receiver is enabled ($\overline{RE}$=L)

Table 9-2. Type 2 Receiver Input Threshold Test Voltage

Applied Voltages		Resulting Differential Input Voltage	Resulting Common-Mode Input Voltage	Receiver Output (Note 2)
V_{IA}	V_{IB}	V_{ID}	V_{IC}	
2.400	0.000	2.400	1.200	H
0.000	2.400	-2.400	1.200	L
3.800	3.650	0.150	3.725	H
3.800	3.750	0.050	3.775	L
-1.250	-1.400	0.150	-1.325	H
-1.350	-1.400	0.050	-1.375	L

Note 2: H = High level, L = Low level, output state assumes receiver is enabled ($\overline{RE}$=L)

9.2 Device Functional Modes

Table 9-3. Device function Table

Type 1 Receiver (UM3405)	**Inputs**		**Output**	
	$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**R**	
	$V_{ID} \geq 50$ mV	L	H	
	-50 mV $< V_{ID} < 50$ mV	L	?	
	$V_{ID} \leq -50$ mV	L	L	
	X	H	Z	
	X	Open	Z	
	Open	L	?	
Type 2 Receiver (UM3406)	**Inputs**		**Output**	
	$V_{ID} = V_A - V_B$	**$\overline{RE}$**	**R**	
	$V_{ID} \geq 150$ mV	L	H	
	50 mV $< V_{ID} < 150$ mV	L	?	
	$V_{ID} \leq 50$ mV	L	L	
	X	H	Z	
	X	Open	Z	
	Open	L	L	
Driver	**Input**	**Enable**	**Output**	
	D	**DE**	**A**	**B**
	L	H	L	H
	H	H	H	L
	Open	H	L	H
	X	Open	Z	Z
	X	L	Z	Z

H = High, L = Low, Z = High Impedance, X = Don't Care, ? = Indeterminate

10 Applications Information

10.1 Receiver Input Threshold (Failsafe)

The MLVDS standard defines a type 1 and type 2 receiver. Type 1 receivers include no provisions for failsafe and have their differential input voltage thresholds near zero volts.Type 2 receivers have their differential input voltage thresholds offset from zero volts to detect the absence of a voltage difference. The impact to receiver output by the offset input can be seen in Table 10-1 and Figure 10-1.

10.1 Receiver Input Threshold (Failsafe) (continued)

Table 10-1. Receiver Input Threshold Requirements

Receiver Type	Output Low	Output High
Type 1	-2.4 V ≤ V_{ID} ≤ -0.05 V	0.05 V ≤ V_{ID} ≤ 2.4 V
Type 2	-2.4 V ≤ V_{ID} ≤ 0.05 V	0.15 V ≤ V_{ID} ≤ 2.4 V

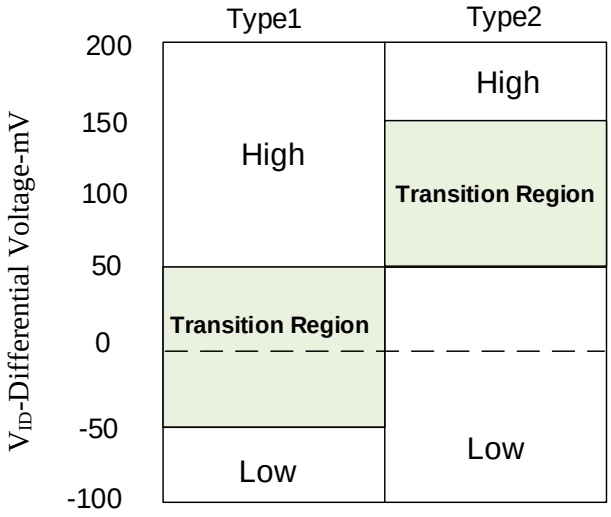


Figure 10-1. Receiver Differential Input Voltage Showing Transition Regions by Type

10.2 Live Insertion/Glitch−Free Power Up/Down

UM3405/3406 provides a glitch-free power up/down feature that prevents the M-LVDS outputs of the device from turning on during a power up or power down event. This is especially important in live insertion applications, when a device is physically connected to an M-LVDS multipoint bus and V_{CC} is ramping. While the M-LVDS interface for these devices is glitch free on power up/down, the receiver output structure is not. The glitch on the R pin is independent of the RE voltage. Any complications or issues from this glitch are easily resolved in power sequencing or system requirements that suspend operation until V_{CC} has reached a steady state value.

Simplex Theory Configurations: Data flow is unidirectional and Point-to-Point from one Driver to one Receiver. UM3405 and UM3406 provide a high signal current allowing long drive runs and high noise immunity. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. See Figures 10-2 and 10-3. UM3405 and UM3406 can be used as the driver or as a receiver.

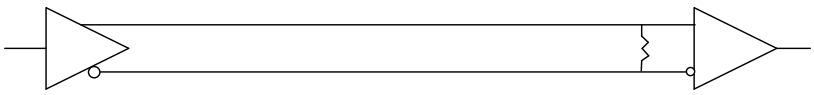


Figure 10-2. Point-to-Point Simplex Single Termination

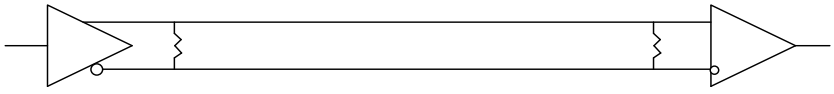


Figure 10-3. Parallel-Terminated Simplex

10.2 Live Insertion/Glitch−Free Power Up/Down (continued)

Simplex Multidrop Theory Configurations: Data flow is unidirectional from one Driver with one or more Receivers Multiple boards required. Single terminated interconnects yield high amplitude levels. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. On the Evaluation Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to a each other or a bus. See Figures 10-4 and 10-5. UM3405 and UM3406 can be used as the driver or as a receiver.

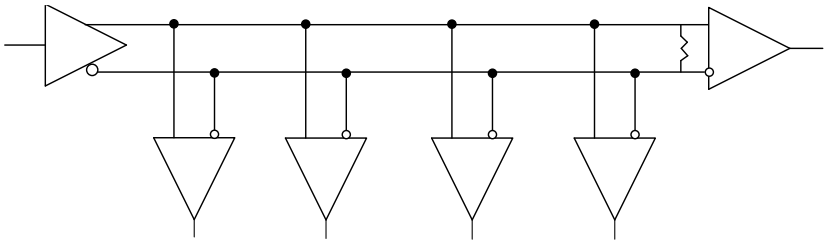


Figure 10-4. Multidrop or Distributed Simplex with Single Termination

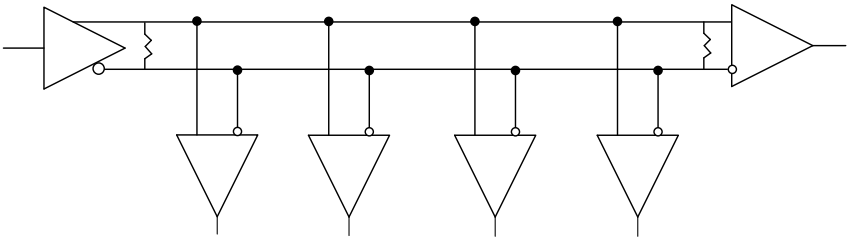


Figure 10-5. Multidrop or Distributed Simplex with Double Termination

Half Duplex Multinode Multipoint Theory Configurations: Data flow is unidirectional and selected from one of multiple possible Drivers to multiple Receivers. One “Two Node” multipoint connection can be accomplished with a single evaluation test board. More than Two Nodes requires multiple evaluation test boards. Parallel terminated interconnects yield typical MLVDS amplitude levels and minimizes reflections. Parallel terminated interconnects yield typical LMVDS amplitude levels and minimizes reflections. On the Test Board, Headers P1, P2, and P3 may be used as need to interconnect transceivers to each other or a bus. See Figure 10-6. UM3406 can be used as the driver or as a receiver.

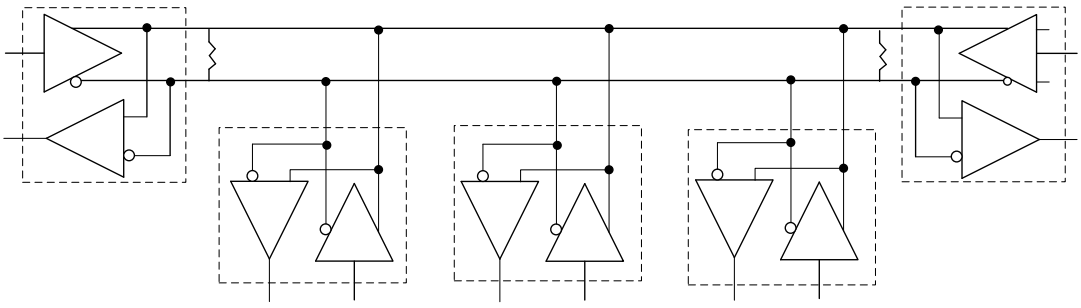
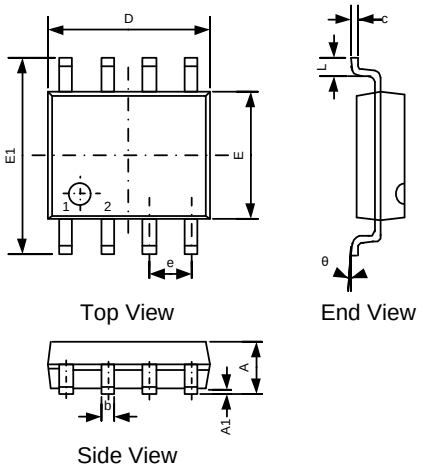


Figure 10-6. Multinode Multipoint Half Duplex (Requires Double Termination)

Package Information

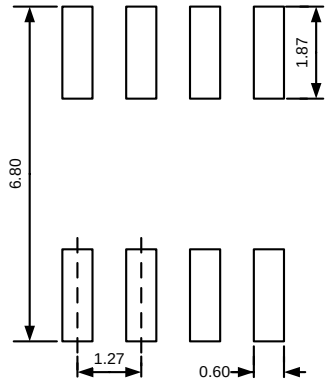
SOP8

Outline Drawing



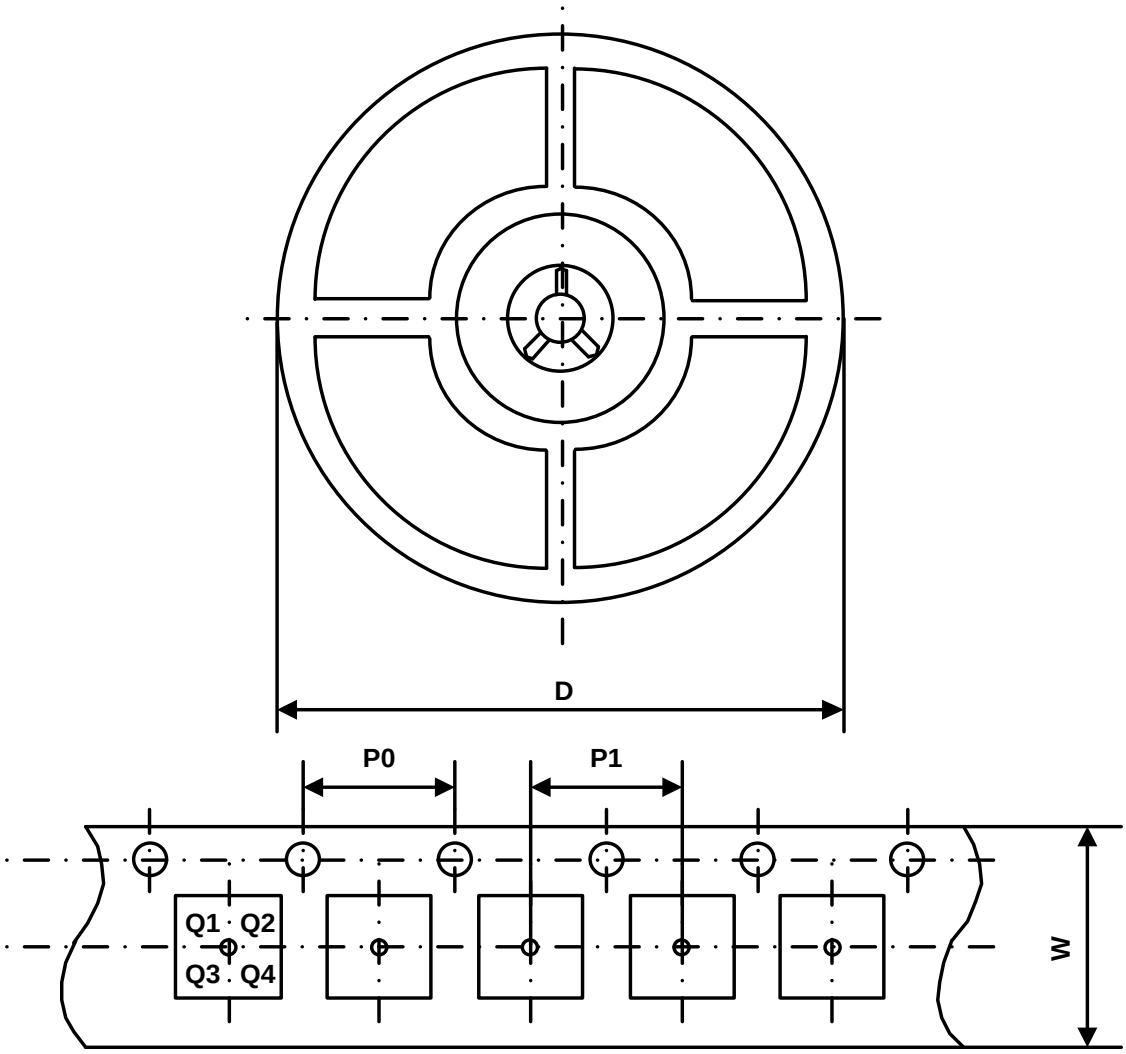
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.75	-	-	0.069
A1	0.00	-	0.25	0.000	-	0.010
b	0.30	-	0.51	0.012	-	0.020
c	0.15	-	0.25	0.006	-	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.70	3.90	4.10	0.148	0.154	0.164
E1	5.80	-	6.25	0.228	-	0.250
e	1.27BSC			0.050 BSC		
L	0.40	-	1.27	0.016	-	0.050
θ	0 °	-	8 °	0 °	-	8 °

Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM3405S8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UM3406S8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1

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