

用于开漏和推挽应用的2位双向电压电平转换器

UM3282FV8 VSSOP8

1 描述

UM3282F 是一款带 ESD 保护的 2 通道电平转换器，可提供允许数据在多压系统中传输所需的电平转换。外部应用电压 V_{CCB} 和 V_{CCA} 用来在器件任一端侧设置逻辑电平。器件 V_{CCA} 端侧的低压逻辑信号在 V_{CCB} 端侧转换为高压逻辑信号，反之亦然。UM3282F 为双向电平转换器，利用基于传输门的设计来允许任意单根数据线上的双向 ($V_{CCA} \leftrightarrow V_{CCB}$) 数据传输。当 $V_{CCA} \leq V_{CCB}$ 时， V_{CCA} 与 V_{CCB} 的工作电压范围同为 +1.1V 至 +5.5V，而当 $V_{CCA} > V_{CCB}$ 时， V_{CCA} 与 V_{CCB} 的工作电压范围则同为 +1.4V 至 +5.5V。

UM3282F 专为采用 I_{OFF} 机制的部分断电应用场景设计。其 I_{OFF} 电路可禁用输出驱动器，从而在器件断电时有效阻止破坏性电流倒灌。其 V_{CC} 隔离特性可确保任一 V_{CC} 输入电源低于 100mV 时，所有电平转换器输出将失效并切换至高阻抗状态。当输出使能 (OE) 为低电平时，UM3282F 进入三态输出模式以降低供电电流。该器件采用由 V_{CCA} 为 OE 输入电路供电的设计，并在信号端提供双向 $\pm 8kV$ ESD 防护，在外部信号切换应用场合提供更强的保护。

UM3282F 采用 VSSOP8 封装。

2 应用

- SPI、MICROWIRE 和 I²C 电平转换
- 手持设备
- 智能手机
- 平板电脑
- 台式计算机

3 特性

- 最大数据速率
 - 100Mbps (推挽, 1.8V 至 3.3V)
 - 2Mbps (开漏)
- V_{CCA} 与 V_{CCB} 独立供电: V_{CCA} 可大于、等于或小于 V_{CCB}
- I_{OFF} 支持局部断电模式运行
- V_{CC} 隔离特性—如果任何一个 V_{CC} 输入接地 (GND), 则两个端口均处于高阻抗状态
- 无需方向控制信号
- 无上电时序要求, V_{CCA} 或 V_{CCB} 均可优先上电
- 低功耗
- A/B 端口 ESD 防护:
 - $\pm 8kV$ 人体放电模型 (HBM)
- 闩锁性能 (Latch-Up) 超过 200mA

4 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UM3282FV8	VJ	VSSOP8	3000pcs/7Inch Tape & Reel

5 Pin Configuration and Function

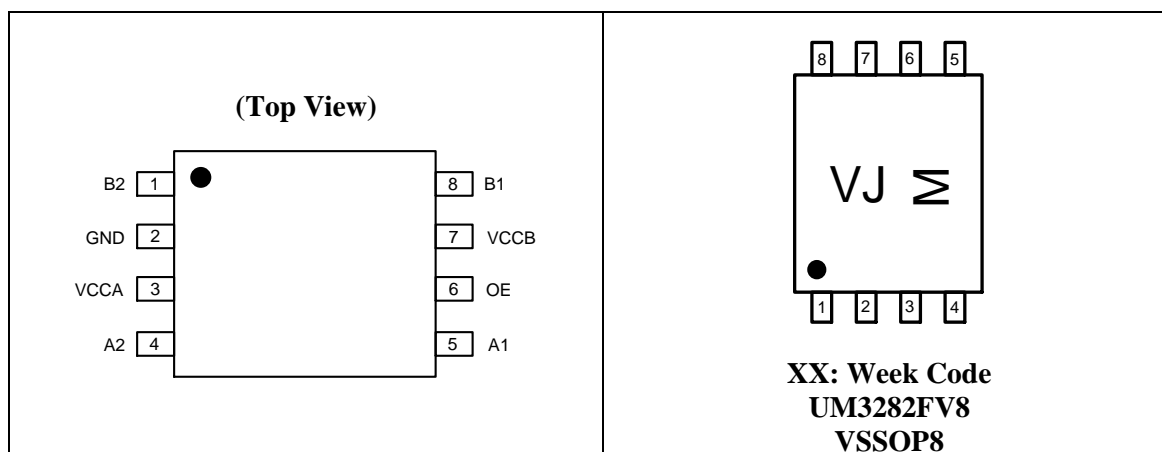


Table 5-1. Pin Functions

Pin No.	Pin Name	Function
1	B2	Input/output 2. Referenced to V_{CCB} .
2	GND	Ground.
3	VCCA	A-Port supply voltage $1.1V \leq V_{CCA} \leq 5.5V$.
4	A2	Input/output 2. Referenced to V_{CCA} .
5	A1	Input/output 1. Referenced to V_{CCA} .
6	OE	3-state output enable input. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA} .
7	VCCB	B-Port supply voltage. $1.1V \leq V_{CCB} \leq 5.5V$
8	B1	Input/output 1. Referenced to V_{CCB} .

6 Specifications

6.1 Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
V _{CCA}	Supply Voltage Range		-0.5 to +6.5	V
V _{CCB}	Supply Voltage Range		-0.5 to +6.5	V
V _I	Input Voltage Range	A ports	-0.5 to +6.5	V
		B ports	-0.5 to +6.5	
V _O	Voltage Range applied to any output in the high-impedance or power-off state	A ports	-0.5 to +6.5	V
		B ports	-0.5 to +6.5	
V _O	Voltage Range applied to any output in the high or low state (Note 2)	A ports	-0.5 to (V _{CCA} +0.5)	V
		B ports	-0.5 to (V _{CCB} +0.5)	
V _{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins	±8	kV
I _{IK}	Input Clamp Current	V _I <0	-50	mA
I _{OK}	Output Clamp Current	V _O <0	-50	mA
I _O	Continuous Output Current		±50	mA
	Continuous Current through V _{CCA} , V _{CCB} , or GND		±100	
T _{OP}	Operating Temperature Range		-40 to +125	°C
T _J	Junction Temperature Range		-40 to +150	°C
T _{STG}	Storage Temperature Range		-65 to +150	°C

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: Maximum voltage must not exceed 6.5V.

6.2 Recommended Operating Conditions (Note 1, 2)

Symbol	Parameter		V _{CCA}	V _{CCB}	Min	Max	Unit
V _{CCA}	Supply Voltage		V _{CCA} ≤ V _{CCB}		1.1	5.5	V
V _{CCB}					1.1	5.5	
V _{CCA}	Supply Voltage		V _{CCA} > V _{CCB}		1.4	5.5	
V _{CCB}					1.4	5.5	
V _{IH}	High Level Input Voltage	A- Port	1.1V to 1.95V	1.1V to 5.5V	V _{CCI} -0.2	V _{CCI}	
			1.95V to 5.5V		V _{CCI} -0.4	V _{CCI}	
		B- Port	1.1V to 5.5V	1.1V to 1.95V	V _{CCI} -0.2	V _{CCI}	
					1.95V to 5.5V	V _{CCI} -0.4	V _{CCI}
		OE	1.1V to 5.5V	1.1V to 5.5V	V _{CCA} ×0.65	5.5	
V _{IL}	Low Level Input Voltage	A- Port	1.1V to 5.5V	1.1V to 5.5V	0	0.15	
		B- Port			0	0.15	
		OE			0	V _{CCA} ×0.35	
Δt/Δv	Input Transition Rise or Fall Time	A-Port push-pull driving	1.1V to 5.5V	1.1V to 5.5V		10	ns/V
		B-Port push-pull driving				10	
		Control input				10	

Note1. V_{CCI} is the supply voltage associated with the input port.

Note2. V_{CCO} is the supply voltage associated with the output port.

6.3 Thermal Information

Symbol	Parameter		Value	Unit
R _{θJA}	Junction-to-ambient thermal resistance	VSSOP8	199.1	°C/W
R _{θJC(TOP)}	Junction-to-case (top) thermal resistance	VSSOP8	72.4	°C/W
R _{θJB}	Junction-to-board thermal resistance	VSSOP8	77.8	°C/W

6.4 Electrical Characteristics

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Test Conditions	V _{CCA}	V _{CCB}	Min	Typ	Max	Unit	
V _{OHA}	I _{OH} =-20μA V _{IB} ≥V _{CCB} -0.2V	1.1V to 5.5V	1.1V to 5.5V	V _{CCA} × 0.67	V _{CCA} -0.1		V	
V _{OLA}	I _{OL} =20uA, V _{IB} ≤0.15V	1.1V to 5.5V	1.1V to 5.5V			0.4	V	
	I _{OL} =180uA, V _{IB} ≤0.15V	1.4V	1.4V to 5.5V			0.4		
	I _{OL} =220uA, V _{IB} ≤0.15V	1.65V	1.4V to 5.5V			0.4		
	I _{OL} =300uA, V _{IB} ≤0.15V	2.3V	1.4V to 5.5V			0.4		
	I _{OL} =400uA, V _{IB} ≤0.15V	3V	1.4V to 5.5V			0.55		
	I _{OL} =620uA, V _{IB} ≤0.15V	4.5V	1.4V to 5.5V			0.55		
V _{OHB}	I _{OH} =-20μA V _{IA} ≥V _{CCA} -0.2V	1.1V to 5.5V	1.1V to 5.5V	V _{CCB} × 0.67	V _{CCB} -0.1		V	
V _{OLB}	I _{OL} =20uA, V _{IA} ≤0.15V	1.1V to 5.5V	1.1V to 5.5V			0.4	V	
	I _{OL} =180uA, V _{IA} ≤0.15V	1.4V to 5.5V	1.4V			0.4		
	I _{OL} =220uA, V _{IA} ≤0.15V	1.4V to 5.5V	1.65V			0.4		
	I _{OL} =300uA, V _{IA} ≤0.15V	1.4V to 5.5V	2.3V			0.4		
	I _{OL} =400uA, V _{IA} ≤0.15V	1.4V to 5.5V	3V			0.55		
	I _{OL} =620uA, V _{IA} ≤0.15V	1.4V to 5.5V	4.5V			0.55		
I _I	OE	V _I =V _{CCI} or GND	1.1V to 5.5V	1.1V to 5.5V	-2	2	μA	
I _{OZ}	A or B Port	OE=V _{IL} V _I =V _{CCI} or GND	1.1V to 5.5V	1.1V to 5.5V	-2	2	μA	
I _{OFF}	A or B Port	V _I or V _O = 0 to 5.5V	0V	0V to 5.5V	-5	0.1	5	μA
			0V to 5.5V	0V	-5	0.1	5	
I _{CCA}	V _I =V _O =open, I _O =0	1.1V to 5.5V	1.1V to 5.5V		2	6	μA	
		5.5V	0V			3		
		0V	5.5V			1		
I _{CCB}	V _I =V _O =open, I _O =0	1.1V to 5.5V	1.1V to 5.5V			12	μA	
		5.5V	0V			1		
		0V	5.5V			3		
I _{CCA} + I _{CCB}	V _I =V _O =open, I _O =0	1.1V to 5.5V	1.1V to 5.5V			18	μA	
I _{CCZA}	V _I =V _O =open, I _O =0, OE=GND	1.1V to 5.5V	1.1V to 5.5V			2	μA	
I _{CCZB}	V _I =V _O =open, I _O =0, OE=GND	1.1V to 5.5V	1.1V to 5.5V			5	μA	
C _I	OE	3.3V	3.3V			5.5	pF	
C _{IO}	A Port					7	pF	
	B Port	3.3V	3.3V			6		

Note 1. When V_{CCA} > V_{CCB}, the recommended voltage range for V_{CCA} and V_{CCB} is from 1.4V to 5.5V.

6.5 Switching Characteristics (Note 1, 2)

Over recommended operating free-air temperature range, $V_{CCA} = 1.2 \pm 0.1V$ (unless otherwise noted).

Parameter	Test Conditions		$V_{CCB} (V)$						Unit					
			1.2±0.1	1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Typ	Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	28	30		30		40		50		70	ns	
		O-D	23	4	25	4	25	3.6	30	3.5	40	3.5		45
t_{PLH}	A-B	P-P	32	25		25		25		30		35	ns	
		O-D	950	190	820	182	720	143	554	114	473	81		384
t_{PHL}	B-A	P-P	28	25		25		25		20		25	ns	
		O-D	23	4	26	3.4	25	3.1	25	2.8	20	2.5		20
t_{PLH}	B-A	P-P	32	35		30		30		25		25	ns	
		O-D	950	190	850	186	745	147	603	118	519	84		407
t_{EN}	OE-A	P-P	0.25	0.2		0.2		0.2		0.2		0.2	us	
	OE-B	P-P	0.25	0.2		0.2		0.2		0.2		0.2	us	
t_{DIS}	OE-A OE-B	P-P	0.2	0.4		0.4		0.4		0.4		0.4	us	
t_{RA}	A port rise time	P-P	37	3	50	3.5	45	3	40	3.1	40	3.2	40	ns
		O-D	702	135	1050	147	982	115	716	92	592	66	481	
t_{RB}	B port rise time	P-P	37	3	30	2.9	25	1.9	20	0.9	16.1	0.7	2.6	ns
		O-D	712	135	1050	135	1020	91	756	58	653	20	600	
t_{FA}	A port fall time	P-P	37	3	40	2.3	35	1.7	30	1.6	30	1.7	30	ns
		O-D	21.5	3	40	2.4	35	2.1	30	1.7	30	1.5	30	
t_{FB}	B port fall time	P-P	36	3	40	2	35	1.3	35	0.9	40	0.8	55	ns
		O-D	22	3	30	1.2	25	1.3	25	1	26	0.5	32	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1	1		1		1		1.1		1	ns	
Max data rate	A to B	P-P	8	30		30		15		12		5	Mbps	
		O-D	0.8	0.8		0.8		0.8		0.8		0.8		
Max data rate	B to A	P-P	8	10		10		10		10		8	Mbps	
		O-D	0.8	0.8		0.8		0.8		0.8		0.8		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

6.5 Switching Characteristics (Note 1, 2) (continued)

 Over recommended operating free-air temperature range, $V_{CCA} = 1.5V \pm 0.1V$ (unless otherwise noted).

Parameter	Test Conditions		V_{CCB} (V)					Unit					
			1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	20		15		13		12		12		ns
		O-D	4	20	4	15.5	3.6	12.8	3.5	12.2	3.5	12	
t_{PLH}	A-B	P-P	15		12		10		9.8		9.7		ns
		O-D	190	820	182	720	143	554	114	473	81	384	
t_{PHL}	B-A	P-P	20		15		13		12		12		ns
		O-D	4	20	3.4	15.5	3.1	14	2.8	15	2.5	14	
t_{PLH}	B-A	P-P	15		12		10		9.8		9		ns
		O-D	190	850	186	745	147	603	118	519	84	407	
t_{EN}	OE-A	P-P	5		0.2		0.2		0.2		0.2		us
	OE-B	P-P	0.2		0.2		0.2		0.2		0.2		us
t_{DIS}	OE-A OE-B	P-P	0.4		0.4		0.4		0.4		0.4		us
t_{RA}	A port rise time	P-P	3	15	3.5	14.5	3	13	3.1	13	3.2	13	ns
		O-D	135	1050	147	982	115	716	92	592	66	481	
t_{RB}	B port rise time	P-P	3	15	2.9	11.4	1.9	7.4	0.9	4.7	0.7	2.6	ns
		O-D	135	1050	135	1020	91	756	58	653	20	370	
t_{FA}	A port fall time	P-P	3	15	2.3	13	1.7	10	1.6	10	1.7	9	ns
		O-D	3	15	2.4	12	2.1	11	1.7	11	1.5	10	
t_{FB}	B port fall time	P-P	3	15	2	13	1.3	8.5	0.9	8.5	0.8	5.1	ns
		O-D	3	15	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1		1		1		1.1		1		ns
Max data rate	A to B	P-P	50		70		100		100		90		Mbps
		O-D	2		2		2		2		2		
Max data rate	B to A	P-P	50		50		50		50		50		Mbps
		O-D	2		2		2		2		2		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

6.5 Switching Characteristics (Note 1, 2) (continued)

 Over recommended operating free-air temperature range, $V_{CCA} = 1.8V \pm 0.15V$ (unless otherwise noted).

Parameter	Test Conditions		V_{CCB} (V)					Unit					
			1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	20		13		10		10		8		ns
		O-D	4	20	3.6	13.5	3.2	11	3.1	11.1	3.1	10	
t_{PLH}	A-B	P-P	15		9		10		6.5		6.3		ns
		O-D	190	820	194	729	155	584	126	466	90	346	
t_{PHL}	B-A	P-P	20		13		10		10		9		ns
		O-D	4	20	3.4	13.5	2.8	12	2.5	12.5	2.1	11	
t_{PLH}	B-A	P-P	15		10.2		10		10		7		ns
		O-D	190	850	197	733	159	578	129	459	93	323	
t_{EN}	OE-A	P-P	30		5		0.2		0.2		0.2		us
	OE-B	P-P	0.2		0.2		0.2		0.2		0.2		us
t_{DIS}	OE-A OE-B	P-P	0.4		0.4		0.4		0.4		0.4		us
t_{RA}	A port rise time	P-P	3	15	3.1	11.9	2.6	10	2.7	10	2.8	9	ns
		O-D	135	1050	155	996	124	691	100	508	72	350	
t_{RB}	B port rise time	P-P	3	15	2.8	10.5	1.8	7.2	1.2	5.2	0.7	2.7	ns
		O-D	135	1050	132	1001	106	677	73	546	32	323	
t_{FA}	A port fall time	P-P	3	15	2.1	12	1.6	10	1.4	7.5	1.4	7	ns
		O-D	3	15	2.2	10	1.7	10	1.4	8.8	1.2	7.5	
t_{FB}	B port fall time	P-P	3	15	2	12	1.3	10	0.9	3.9	0.7	3	ns
		O-D	3	15	0.8	10.5	0.7	10.7	1	9.6	0.6	5.1	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1		1		1		1		1		ns
Max data rate	A to B	P-P	50		70		100		100		100		Mbps
		O-D	2		2		2		2		2		
Max data rate	B to A	P-P	70		70		75		75		75		Mbps
		O-D	2		2		2		2		2		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

6.5 Switching Characteristics (Note 1, 2) (continued)

 Over recommended operating free-air temperature range, $V_{CCA} = 2.5V \pm 0.2V$ (unless otherwise noted).

Parameter	Test Conditions		V_{CCB} (V)					Unit					
			1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	20		13		8		7		6.5		ns
		O-D	4	20	3.6	13.5	2.4	10	2.3	8.8	2.2	8.2	
t_{PLH}	A-B	P-P	15		9		6		5		4.5		ns
		O-D	190	820	194	729	149	592	125	488	93	368	
t_{PHL}	B-A	P-P	20		13		9.4		7.5		7.0		ns
		O-D	4	20	3.4	13.5	2.5	10	2.2	9	1.8	8.5	
t_{PLH}	B-A	P-P	15		10.2		5.9		5.6		4.8		ns
		O-D	190	850	197	733	150	595	126	481	94	345	
t_{EN}	OE-A	P-P	50		30		5		0.2		0.2		us
	OE-B	P-P	0.3		0.2		0.2		0.2		0.2		us
t_{DIS}	OE-A OE-B	P-P	0.4		0.4		0.4		0.4		0.4		us
t_{RA}	A port rise time	P-P	3	15	3.1	11.9	2	7.3	2.1	6.4	2.2	5.8	ns
		O-D	135	1050	155	996	110	692	93	529	68	411	
t_{RB}	B port rise time	P-P	3	15	2.8	10.5	1.8	6.5	1.3	5.1	0.7	3.4	ns
		O-D	135	1050	132	1001	107	693	79	520	41	353	
t_{FA}	A port fall time	P-P	3	15	2.1	10	1.5	5.7	1.2	4.9	1.3	4.5	ns
		O-D	3	15	2.2	10	1.5	6.6	1.2	5.2	1.1	4.5	
t_{FB}	B port fall time	P-P	3	15	2	10	1.4	6.3	0.9	4.1	0.7	3	ns
		O-D	3	15	0.8	10	0.4	6.5	0.5	5.4	0.4	3	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1		1		1		1.2		1		ns
Max data rate	A to B	P-P	50		80		100		100		100		Mbps
		O-D	2		2		2		2		2		
Max data rate	B to A	P-P	100		100		100		100		100		Mbps
		O-D	2		2		2		2		2		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

6.5 Switching Characteristics (Note 1, 2) (continued)

 Over recommended operating free-air temperature range, $V_{CCA} = 3.3V \pm 0.3V$ (unless otherwise noted).

Parameter	Test Conditions		V_{CCB} (V)					Unit					
			1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	20		13		8		6.8		5.5		ns
		O-D	4	20	3.6	13.5	2.4	10	2	8.5	1.9	7.8	
t_{PLH}	A-B	P-P	15		9		6		4.3		3.9		ns
		O-D	190	820	194	729	149	592	111	439	87	352	
t_{PHL}	B-A	P-P	20		13		9.4		7.5		6.8		ns
		O-D	4	20	3.4	13.5	2.5	10	2.1	8.8	1.7	7.8	
t_{PLH}	B-A	P-P	15		10.2		5.9		5.1		4.3		ns
		O-D	190	850	197	733	150	595	112	449	86	339	
t_{EN}	OE-A	P-P	50		30		30		5		0.2		us
	OE-B	P-P	0.4		0.3		0.2		0.2		0.2		us
t_{DIS}	OE-A OE-B	P-P	0.4		0.4		0.4		0.4		0.4		us
t_{RA}	A port rise time	P-P	3	4	3.1	4	2	4	1.8	4.5	1.9	5	ns
		O-D	135	1050	155	996	110	692	75	580	57	488	
t_{RB}	B port rise time	P-P	3	15	2.8	10.5	1.8	6.5	1.5	5	1	3.6	ns
		O-D	135	1050	132	1001	107	693	72	580	40	485	
t_{FA}	A port fall time	P-P	3	5	2.1	5	1.5	5	1.2	4.5	1.1	3.5	ns
		O-D	3	5	2.2	5	1.5	5	1.1	4.4	1	3.7	
t_{FB}	B port fall time	P-P	3	10	2	10	1.4	5	1.1	4.2	0.8	3.1	ns
		O-D	3	10	0.8	10	0.4	5	1	4.2	0.8	3.1	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1		1		1		1		1		ns
Max data rate	A to B	P-P	50		70		100		100		100		Mbps
		O-D	2		2		2		2		2		
Max data rate	B to A	P-P	100		100		100		100		100		Mbps
		O-D	2		2		2		2		2		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

6.5 Switching Characteristics (Note 1, 2) (continued)

 Over recommended operating free-air temperature range, $V_{CCA} = 5V \pm 0.5V$ (unless otherwise noted).

Parameter	Test Conditions		V_{CCB} (V)					Unit					
			1.5±0.1		1.8±0.15		2.5±0.2		3.3±0.3		5±0.5		
			Min	Max	Min	Max	Min		Max	Min	Max	Min	Max
t_{PHL}	A-B	P-P	20		13		8		6.8		5.5		ns
		O-D	4	20	3.6	13.5	2.4	10	2	8.5	1.9	7.8	
t_{PLH}	A-B	P-P	15		9		6		4.3		3.9		ns
		O-D	190	820	194	729	149	592	111	439	87	352	
t_{PHL}	B-A	P-P	15		13		9.4		7.5		6.8		ns
		O-D	4	15	3.4	13.5	2.5	10	2.1	8.8	1.7	7.8	
t_{PLH}	B-A	P-P	15		10.2		5.9		5.1		4.3		ns
		O-D	190	850	197	733	150	595	112	449	86	339	
t_{EN}	OE-A	P-P	130		50		50		30		5		us
	OE-B	P-P	0.4		0.4		0.2		0.2		0.2		us
t_{DIS}	OE-A OE-B	P-P	0.4		0.4		0.4		0.4		0.4		us
t_{RA}	A port rise time	P-P	3	4	3.1	4	1	2	1	2	1	2	ns
		O-D	135	1050	155	996	110	692	75	580	57	488	
t_{RB}	B port rise time	P-P	3	15	2.8	10.5	1.8	6.5	1.5	5	1	3.6	ns
		O-D	135	1050	132	1001	107	693	72	580	40	485	
t_{FA}	A port fall time	P-P	3	5	2.1	5	1.5	3	1.2	3.1	1.1	3.5	ns
		O-D	3	5	2.2	5	1.5	3	1.1	3.1	1	3.7	
t_{FB}	B port fall time	P-P	3	10	2	10	1.4	5	1.1	3.2	0.8	3.1	ns
		O-D	3	10	0.8	10	0.4	5	1	3.2	0.8	3.1	
$t_{SK(O)}$	Channe l-to-Ch annel	P-P	1		1		1		1		1		ns
Max data rate	A or B	P-P	50		70		100		100		100		Mbps
		O-D	2		2		2		2		2		
Max data rate	B to A	P-P	100		100		100		100		100		Mbps
		O-D	2		2		2		2		2		

Note 1: P-P means push-pull; O-D means Open-drain.

Note 2: The duty cycle of the output signal ranges from 40% to 60%.

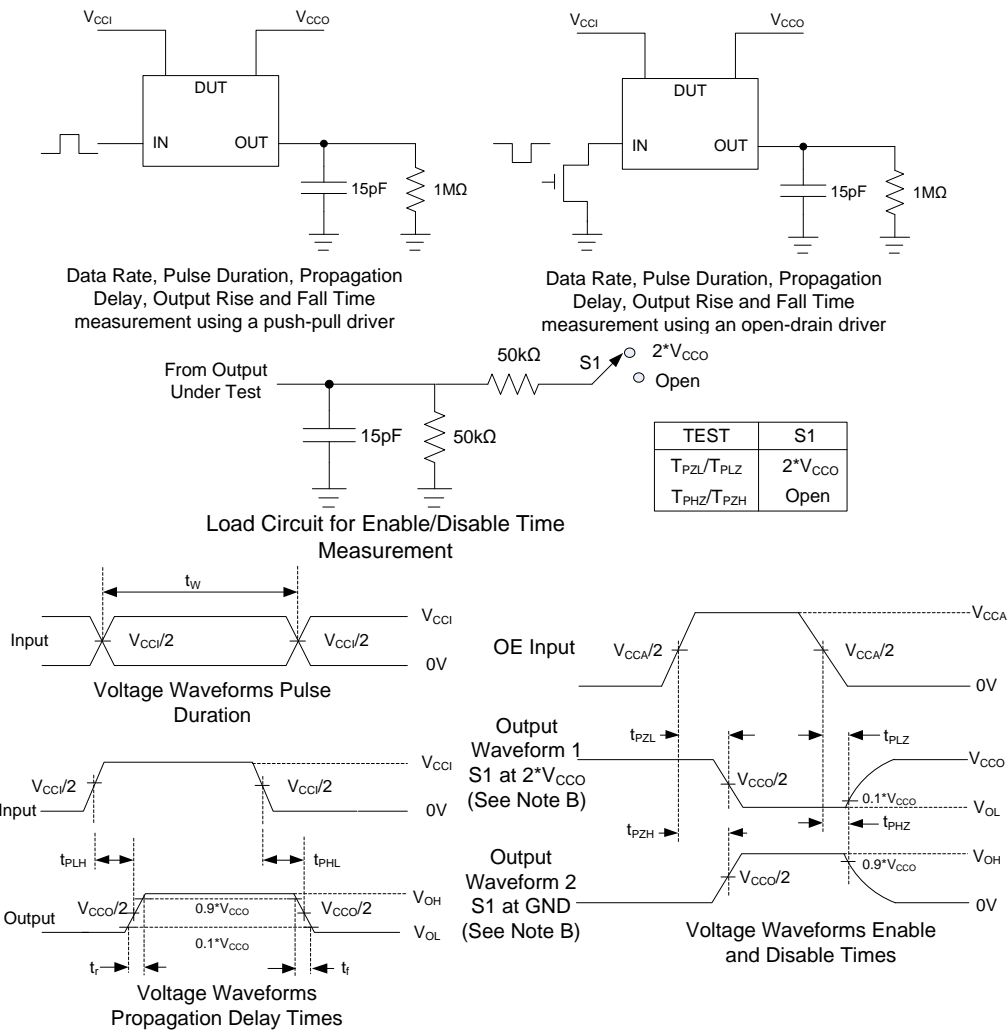
6.6 Operating Characteristics: $V_{CCA} = 1.5\text{ V to }2.5\text{ V}$, $V_{CCB} = 1.5\text{ V to }2.5\text{ V}$ $T_A = 25^\circ\text{C}$.

Parameter	Test Conditions		$V_{CCA}=1.5\text{V}$, $V_{CCB}=1.5\text{V}$			$V_{CCA}=1.8\text{V}$, $V_{CCB}=1.8\text{V}$			$V_{CCA}=2.5\text{V}$, $V_{CCB}=2.5\text{V}$			Unit
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
C_{PDA}	$C_L = 0$, $f = 10\text{ MHz}$, $t_R = t_F = 1\text{ ns}$, $OE = V_{CCA}$ (outputs enabled)	A-port input, B-port output	10			12			16			pF
		B-port input, A-port output	11			13			18			
C_{PDB}		A-port input, B-port output	11			13			18			
		B-port input, A-port output	10			12			16			

6.6 Operating Characteristics (continued): $V_{CCA} = 3.3\text{V to }5.0\text{ V}$, $V_{CCB} = 3.3\text{V to }5.0\text{ V}$ $T_A = 25^\circ\text{C}$.

Parameter	Test Conditions		$V_{CCA}=3.3\text{V}$, $V_{CCB}=3.3\text{V}$			$V_{CCA}=5.0\text{V}$, $V_{CCB}=5.0\text{V}$			Unit
			Min	Typ	Max	Min	Typ	Max	
C_{PDA}	$C_L = 0$, $f = 10\text{ MHz}$, $t_R = t_F = 1\text{ ns}$, $OE = V_{CCA}$ (outputs enabled)	A-port input, B-port output	21			38			pF
		B-port input, A-port output	24			42			
C_{PDB}		A-port input, B-port output	24			42			
		B-port input, A-port output	21			38			

7 Parameter Measurement Information



- A. C_L includes probe and jig capacitances.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{MHz}$, $Z_o = 50\Omega$, $dv/dt \geq 1\text{V/ns}$.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. T_{PLZ} and T_{PHZ} are the same as t_{DIS} .
- F. T_{PZL} and T_{PZH} are the same as t_{EN} .
- G. V_{CCI} is the V_{CC} associated with the input port.
- H. V_{CCO} is the V_{CC} associated with the output port.
- I. All parameters and waveforms are not applicable to all devices.

Figure 7-1. Load Circuits and Voltage Waveforms

8 Detailed Description

8.1 Architecture

The UM3282F is Semi-Buffered Architecture (Figure 8-1). Each channel has edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-pass MOSFET (on the order of 300 Ω to 500 Ω) and pull-up resistors (to provide DC-bias and drive capabilities). In a high state, the N-pass MOSFET switch off and the output can maintain high by R_{PU} . While in a low state, the N-pass MOSFET switch on and the output is driven to low by external driver. In both states, the output is designed to weak, so that they can be overdriven by an external driver when data on the bus starts flowing to the opposite direction.

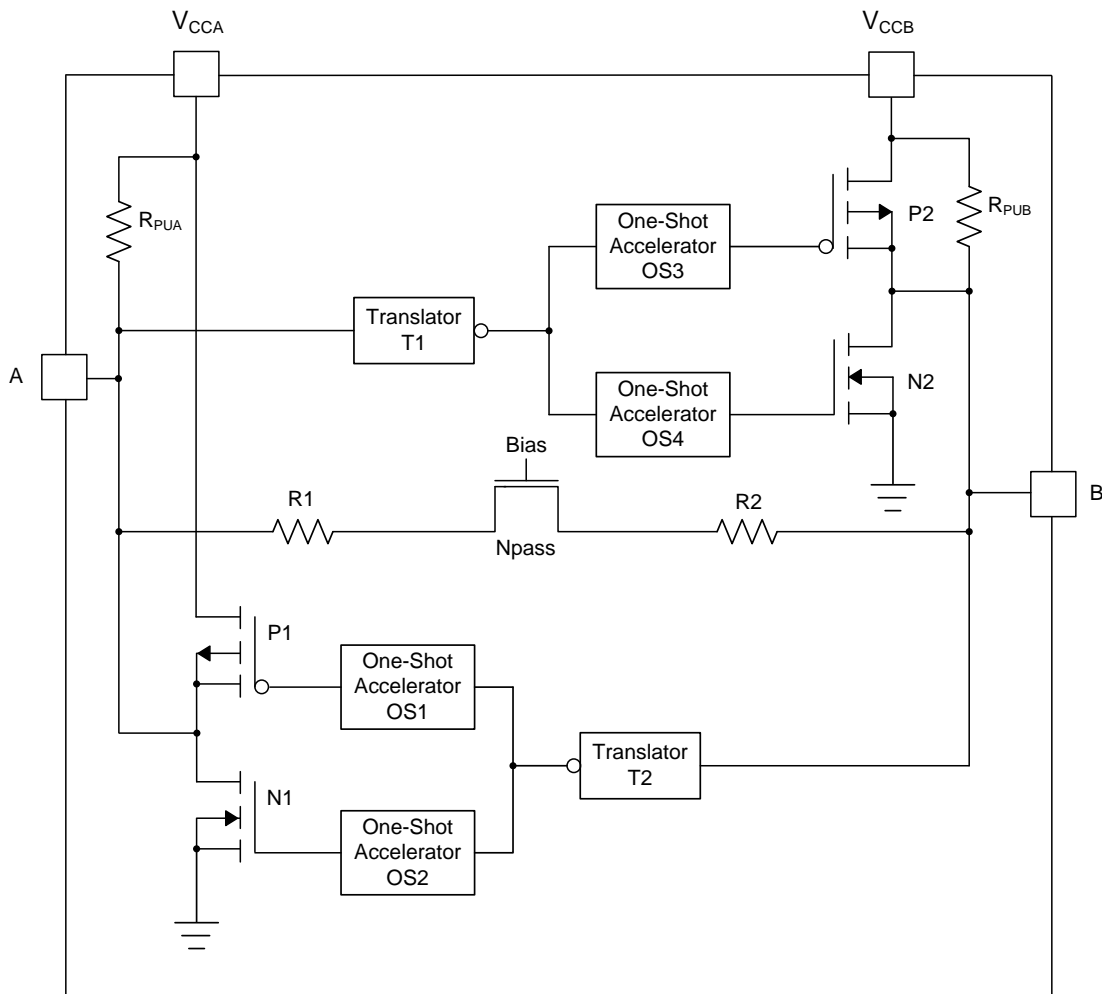


Figure 8-1. Architecture of UM3282F I/O Cell

The output one-shot detects rising or falling edges on the A or B ports. During a rising edge, the one-shot turns on the PMOS transistors (P1, P2) for a short duration, which speeds up the low-to-high transition. Similarly, during a falling edge, the one-shot turns on the NMOS transistors (N1, N2) for a short duration, which speeds up the high-to-low transition.

8.2 Input Driver Requirements

The fall time (t_{FA} , t_{FB}) of a signal depends on the edge-rate and output impedance of the external device driving UM3282F data I/Os, as well as the capacitive loading on the data lines.

Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{FA} , t_{FB} , t_{PHL} , and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω .

8.3 Output Load Considerations

The PCB layout should be practiced carefully with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver.

The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration, also depends on the one-shot output resistance. It is recommended less than 100pF . With very heavy capacitive loads, the one-shot cannot drive fully to the positive rail, retriggering may take place.

8.4 Enable and Disable

The UM3282F has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (t_{DIS}) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (t_{EN}) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

8.5 Pull-up or Pull-down Resistors on I/O Lines

The UM3282F has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB} . R_{PUA} and R_{PUB} have a value of $40\text{k}\Omega$ when the output is driving low. R_{PUA} and R_{PUB} have a value of $4\text{k}\Omega$ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE=Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower V_{OL} values for the same size pass-gate transistor, and helps improve simultaneous switching performance

When an open-drain driver is connected to the data I/Os, Each port is at a low level with an internal pull-up resistance of $40\text{k}\Omega$, that seriously affecting the t_R of the input signal, and the communication speed. It is recommended adding an external pull-up resistor in the input pin that can decrease t_R and improve communication rate. Normally, an additional $4\text{k}\Omega$ pull-up resistor is added to the input side to increase the communication rate by 1Mbps , and so on.

9 Application Information

9.1 Application Information

The UM3282F can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The A-port accepts I/O voltages ranging from 1.1 V to 5.5 V. The B-port accepts I/O voltages from 1.1 V to 5.5 V. The device is ideal for use in application where an open-drain driver is connected to the data I/Os and can also be used in applications where a push-pull driver is connected to the data I/Os. The device has edge rate accelerators (one-shot) to improve the data rate. The pull-up resistors (R_{PU}), commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed.

9.2 Typical Application

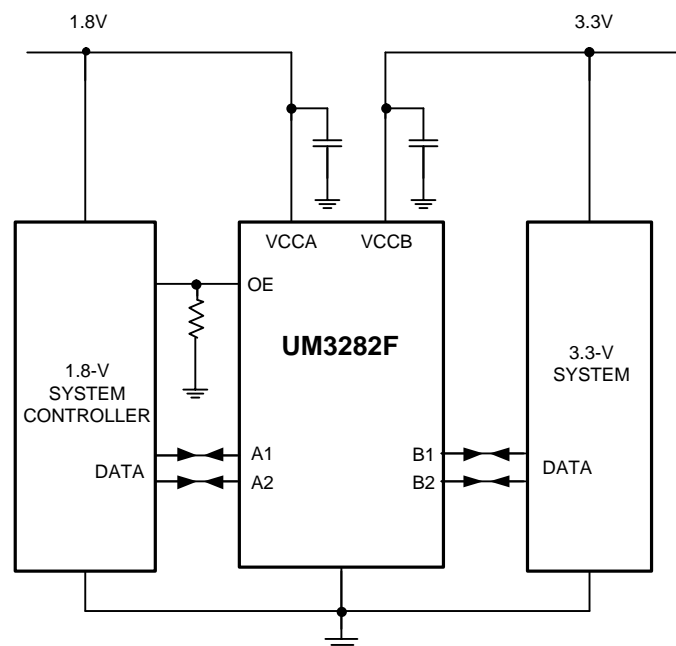
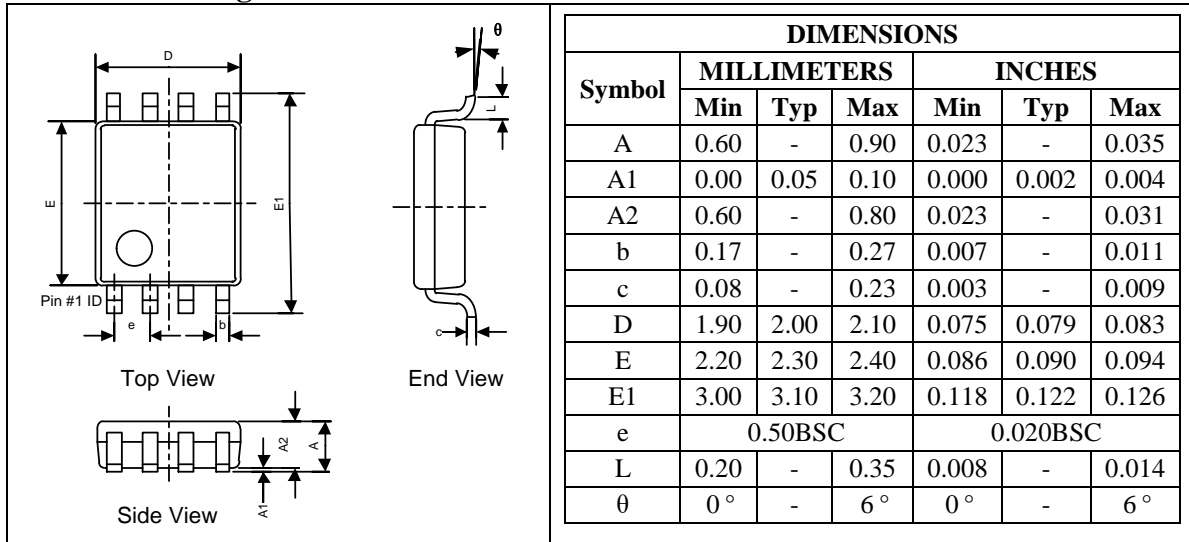


Figure 9-1. UM3282F Typical Application

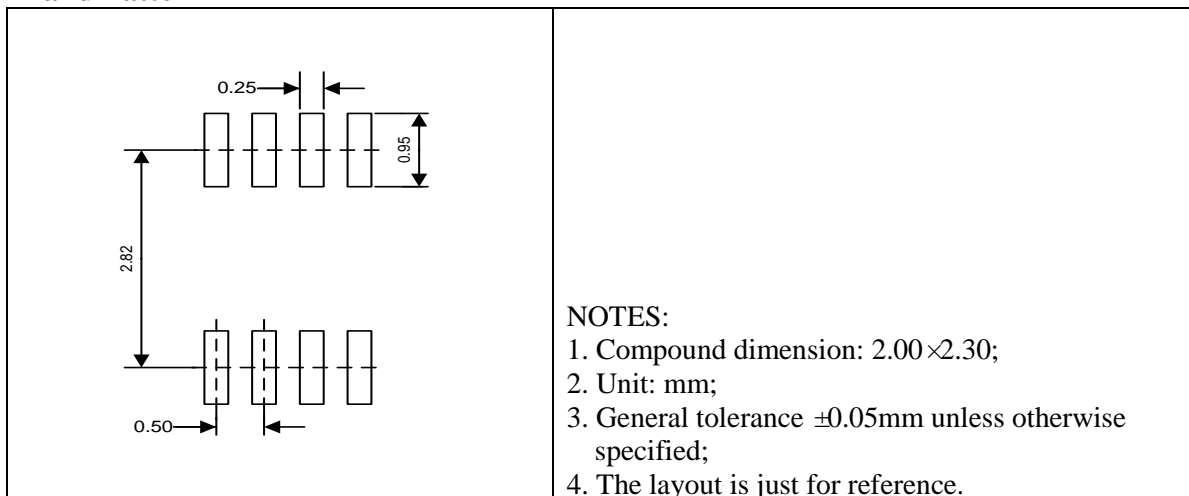
Package Information

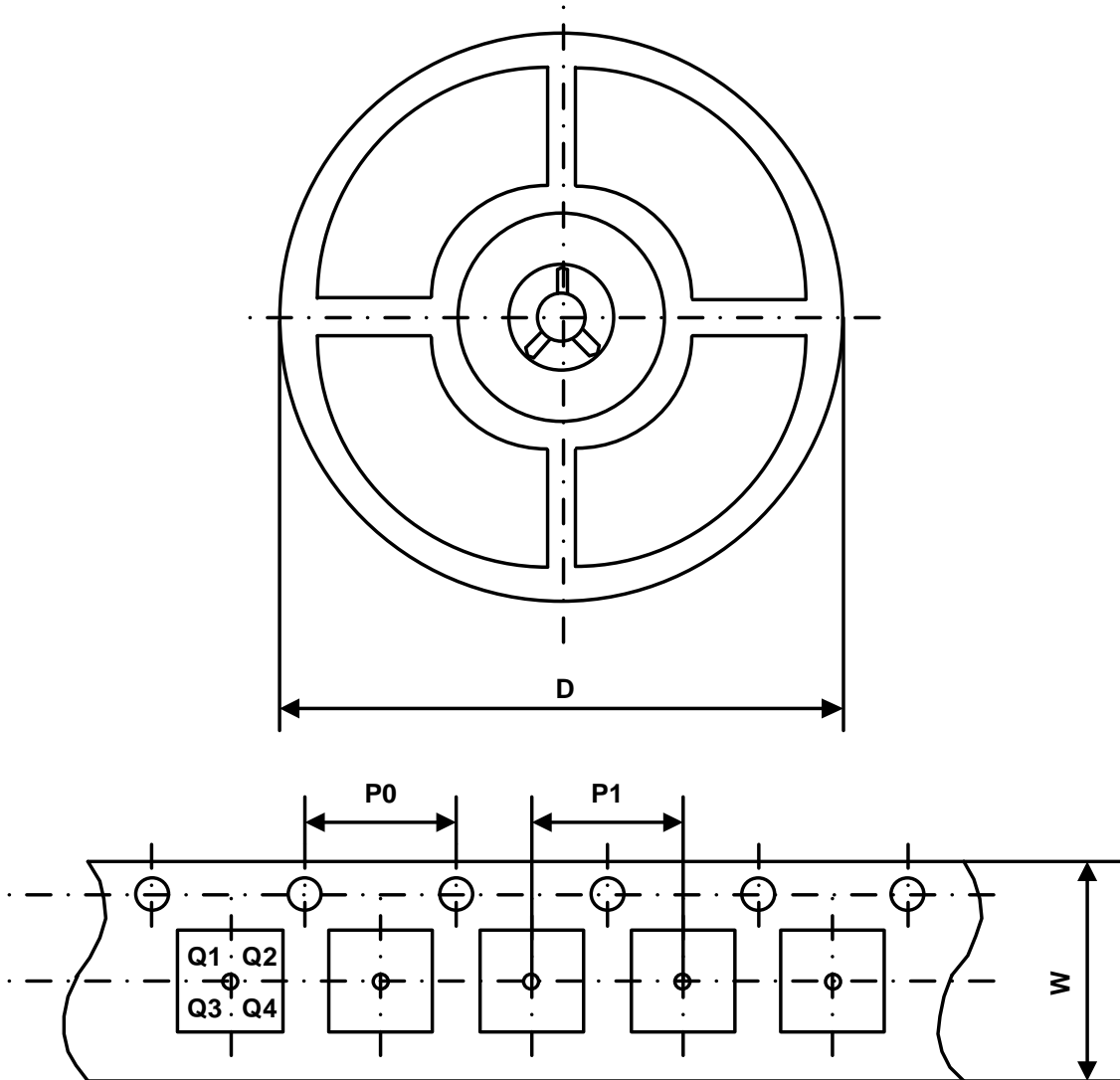
VSSOP8

Outline Drawing



Land Pattern



Packing Information


Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM3282FV8	VSSOP8	8 mm	4 mm	4 mm	180 mm	Q3

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