
High-Speed Six-Channel Digital Isolators

UMISO7760 WSOP16**UMISO7761 WSOP16****UMISO7762 WSOP16****UMISO7763 WSOP16**

1 Description

The UMISO776x series are high-performance six-channel, unidirectional digital isolators with 5kV_{RMS} (wide body package) isolation rating and DC to 150Mbps data rate. The CMTI of the UMISO776x series is up to 200kV/us. The devices feature high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high voltage/current transients from sensitive or human interface circuitry.

The UMISO776x series provides four kinds of direction configuration and two kinds of default output configuration. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H.

The UMISO776x series are available in WSOP16 (wide body package) package. The devices are characterized over ambient free-air temperatures from -40 °C to 125 °C.

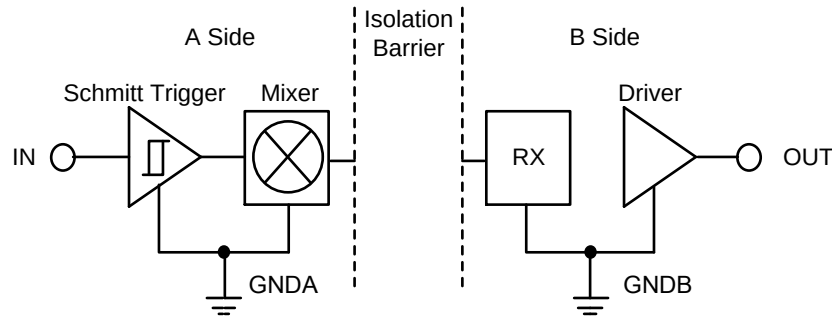
2 Features

- Data rate: DC to 150Mbps
- Robust galvanic isolation of digital signals
 - High lifetime: >40 years
 - Up to 5000 V_{RMS} isolation rating
 - ±200 kV/μs typical CMTI
- Wide supply range: 2.375V to 5.5V
- Extended ambient temperature range: -40 °C to 125 °C
- Available in WSOP16 package
- Default output high (UMISO776xH) and low (UMISO776xL) options
- High Electromagnetic Immunity
- No start-up initialization required
- Excellent propagation delay and skew
 - Propagation delay: < 15ns
 - Pulse width distortion: < 2.6ns
- Compliant with safety regulatory
 - DIN EN IEC 60747-17 (VDE 0884-17)
 - UL according to UL1577
 - IEC 61010-1 and GB 4943.1-2022

3 Applications

- Industrial Automation
- Medical Systems
- Solar Inverter
- Motor Control
- Isolated Power Supplies
- Isolated ADC,DAC

4 Simplified Channel Structure

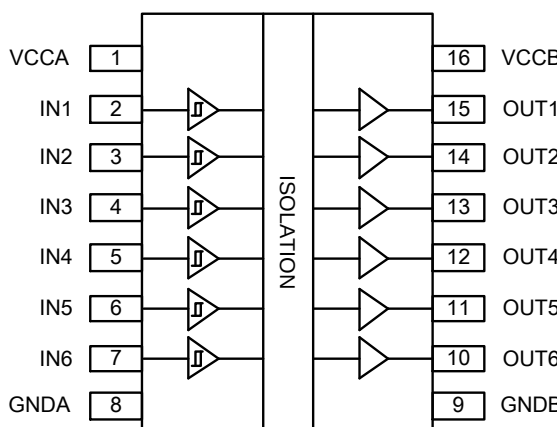
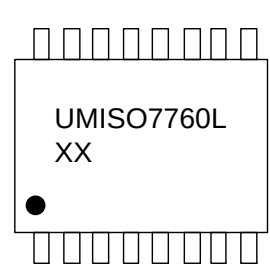
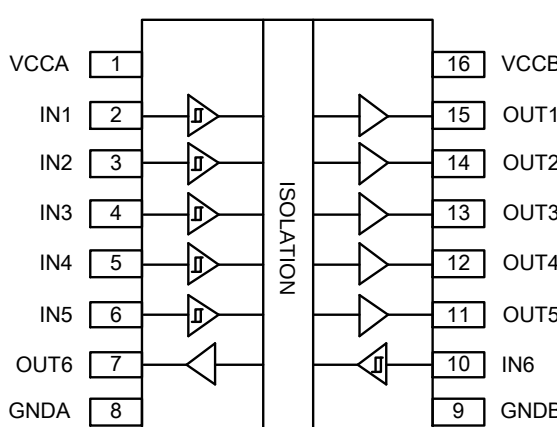
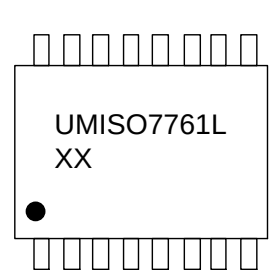
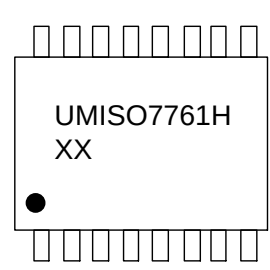


GNDA and GNDB are the isolated grounds for A side and B side respectively.

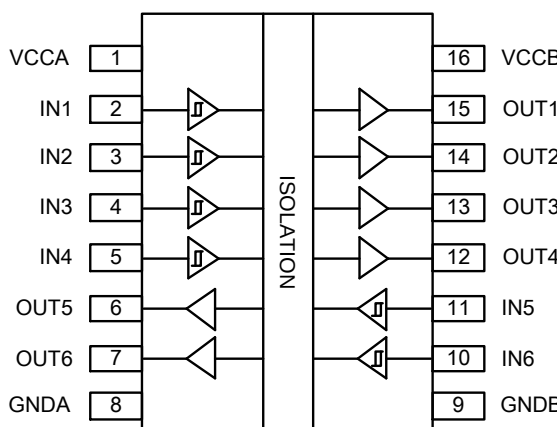
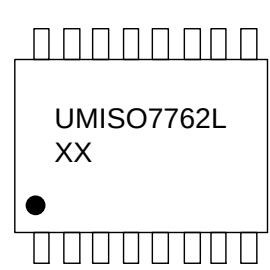
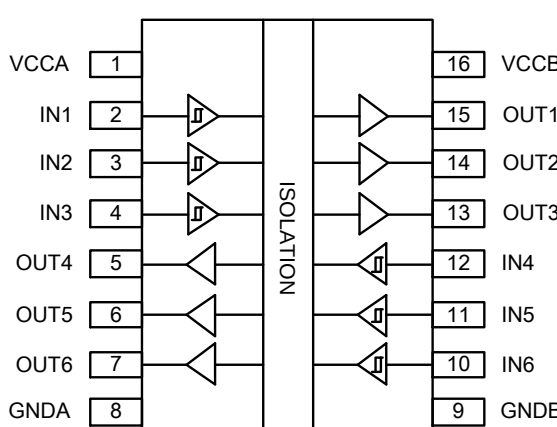
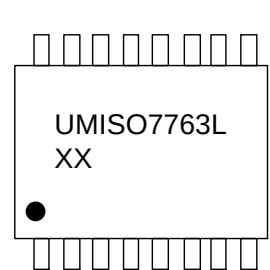
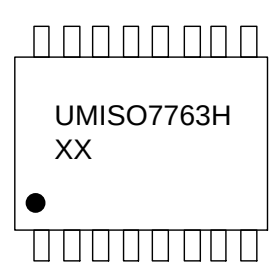
5 Ordering Information

Part Number	A Side Inputs	B Side Inputs	Default Output	Isolation Rating (V _{RMS})	Mark Code	Shipping Qty
UMISO7760LWSG	6	0	Low	5000	UMISO7760L	1500pcs/13Inch Tape & Reel
UMISO7760HWSG	6	0	High	5000	UMISO7760H	1500pcs/13Inch Tape & Reel
UMISO7761LWSG	5	1	Low	5000	UMISO7761L	1500pcs/13Inch Tape & Reel
UMISO7761HWSG	5	1	High	5000	UMISO7761H	1500pcs/13Inch Tape & Reel
UMISO7762LWSG	4	2	Low	5000	UMISO7762L	1500pcs/13Inch Tape & Reel
UMISO7762HWSG	4	2	High	5000	UMISO7762H	1500pcs/13Inch Tape & Reel
UMISO7763LWSG	3	3	Low	5000	UMISO7763L	1500pcs/13Inch Tape & Reel
UMISO7763HWSG	3	3	High	5000	UMISO7763H	1500pcs/13Inch Tape & Reel

6 Pin Configuration and Function

	 UMISO7760L XX XX: Week Code UMISO7760LWSG WSOP16
	 UMISO7761L XX XX: Week Code UMISO7761LWSG WSOP16
	 UMISO7761H XX XX: Week Code UMISO7761HWSG WSOP16

6 Pin Configuration and Function (continued)

	 UMISO7762L XX XX: Week Code UMISO7762LWSG WSOP16
	 UMISO7763L XX XX: Week Code UMISO7763LWSG WSOP16  UMISO7763H XX XX: Week Code UMISO7763HWSG WSOP16

6 Pin Configuration and Function (continued)

Table 6-1. Pin Functions

Pin No.				Pin Name	Function
UMISO7760	UMISO7761	UMISO7762	UMISO7763		
1	1	1	1	VCCA	Power supply for isolator side A.
2	2	2	2	IN1	Logic input 1, corresponds to logic output 1.
3	3	3	3	IN2	Logic input 2, corresponds to logic output 2.
4	4	4	4	IN3	Logic input 3, corresponds to logic output 3.
5	5	5	12	IN4	Logic input 4, corresponds to logic output 4.
6	6	11	11	IN5	Logic input 5, corresponds to logic output 5.
7	10	10	10	IN6	Logic input 5, corresponds to logic output 5.
8	8	8	8	GNDA	Ground reference for isolator side A.
9	9	9	9	GNDB	Ground reference for isolator side B.
10	7	7	7	OUT6	Logic output 6, OUT6 is the logic output for the IN6 input.
11	11	6	6	OUT5	Logic output 5, OUT5 is the logic output for the IN6 input.
12	12	12	5	OUT4	Logic output 4, OUT4 is the logic output for the IN4 input.
13	13	13	13	OUT3	Logic output 3, OUT3 is the logic output for the IN3 input.
14	14	14	14	OUT 2	Logic output 2, OUT2 is the logic output for the IN2 input.
15	15	15	15	OUT 1	Logic output 1, OUT1 is the logic output for the IN1 input.
16	16	16	16	VCCB	Power supply for isolator side B.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CCA}	Supply voltage for isolator side A	Note 2	-0.5		6	V
V _{CCB}	Supply voltage for isolator side B	Note 2	-0.5		6	V
V _I	Voltage on IN _x , OUT _x	Note 3	-0.5		V _{CCX} +0.5	V
V _{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
I _{LU}	Latch up, per JEDEC JESD78			200		mA
I _O	Output current		-15		15	mA
T _J	Junction temperature				150	°C
T _{STG}	Storage temperature		-65		150	°C

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.

Note 3: Maximum voltage must not exceed 6 V.

7.2 Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CCA}	Supply voltage for isolator side A		2.375	3.3/5.0	5.5	V
V _{CCB}	Supply voltage for isolator side B		2.375	3.3/5.0	5.5	V
V _{CC(UVLO+)}	V _{CC} undervoltage-lockout threshold when supply voltage is rising		2	2.2	2.35	V
V _{CC(UVLO-)}	V _{CC} undervoltage-lockout threshold when supply voltage is falling		1.98	2.1	2.21	V
V _{HYS(UVLO)}	V _{CC} undervoltage-lockout threshold hysteresis		100	120	160	mV
I _{OH}	High-level output current	V _{CCO} = 5V (Note 1)	-4			mA
		V _{CCO} = 3.3V	-2			
		V _{CCO} = 2.5V	-1			
I _{OL}	Low-level output current	V _{CCO} = 5V			4	mA
		V _{CCO} = 3.3V			2	
		V _{CCO} = 2.5V			1	

7.2 Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{IH}	Input High Voltage		2			V
V _{IL}	Input Low Voltage				0.8	V
DR	Data rate				150	Mbps
T _A	Ambient temperature		-40	25	125	°C

Note 1: V_{CCO} = Output-side supply V_{CC}.

7.3 Thermal Information

Symbol	Parameter	Value	Unit
R _{θJA}	Junction to ambient thermal resistance	WSOP16 85.5	°C/W

7.4 Power Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7760						
P _D	Maximum power dissipation	V _{CCA} = V _{CCB} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			661	mW
P _{DA}	Maximum power dissipation on A side				81	mW
P _{DB}	Maximum power dissipation on B side				580	mW
UMISO7761						
P _D	Maximum power dissipation	V _{CCA} = V _{CCB} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			661	mW
P _{DA}	Maximum power dissipation on A side				168	mW
P _{DB}	Maximum power dissipation on B side				493	mW
UMISO7762						
P _D	Maximum power dissipation	V _{CCA} = V _{CCB} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			661	mW
P _{DA}	Maximum power dissipation on A side				218	mW
P _{DB}	Maximum power dissipation on B side				443	mW

7.4 Power Rating (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7763						
P _D	Maximum power dissipation	V _{CCA} = V _{CCB} = 5.5 V, C _L = 15 pF, T _J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			661	mW
P _{DA}	Maximum power dissipation on A side				330.5	mW
P _{DB}	Maximum power dissipation on B side				330.5	mW

7.5 Insulation Specifications

Symbol	Parameter	Conditions	Value	Unit
			WSOP16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	16	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	V
	Material group	Per IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V _{RMS}	I-IV	
		Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V _{RMS}	I-II	
DIN V VDE V 0884-17:2021-10 (Note 1)				
V _{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	V _{PK}
V _{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	V _{RMS}
		DC voltage	1414	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (certified); V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% product test)	7070	V _{PK}
V _{IMP}	Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC 62368-1,	6000	V _{PK}
V _{IOSM}	Maximum surge isolation voltage	V _{IOSM} ≥ 1.3 × V _{IMP} ; Tested in oil (qualification test), 1.2/50 μs waveform per IEC 62368-1	8000	V _{PK}

7.5 Insulation Specifications (continued)

Symbol	Parameter	Conditions	Value	Unit
			WSOP16	
q_{pd}	Apparent charge (Note 3)	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.2 \times V_{IORM}$, $t_m = 10$ s	≤ 5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s; $V_{pd(m)} = 1.3 \times V_{IORM}$, $t_m = 10$ s	≤ 5	pC
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, $t_{ini} = 1$ s; $V_{pd(m)} = 1.5 \times V_{IORM}$, $t_m = 1$ s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤ 5	pC
C_{IO}	Barrier capacitance, input to output (Note 4)	$V_{IO} = 0.4 \times \sin(2\pi ft)$, $f = 1$ MHz	~ 1.0	pF
R_{IO}	Isolation resistance (Note 4)	$V_{IO} = 500$ V, $T_A = 25$ °C	$>10^{12}$	Ω
		$V_{IO} = 500$ V, 100 °C $\leq T_A \leq 125$ °C	$>10^{11}$	
		$V_{IO} = 500$ V at $T_s = 150$ °C	$>10^9$	
	Pollution degree		2	
UL 1577				
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, $t = 60$ s(qualification) $V_{TEST} = 1.2 \times V_{ISO}$, $t = 1$ s (100% production test)	5000	V_{RMS}

Note 1: This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

Note 2: Devices are immersed in oil during surge characterization test.

Note 3: The characterization charge is discharging charge (pd) caused by partial discharge.

Note 4: Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.6 Electrical Characteristics

7.6.1 Electrical Characteristics ($V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$I_{OH} = -4\text{ mA}$ (Note 1)	$V_{CCO} - 0.4$	4.8		V
V_{OL}	Output low voltage	$I_{OL} = 4\text{ mA}$		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	$V_{IH} = V_{CCA}$ at IN_x			20	μA
I_{IL}	Low-level input leakage current	$V_{IL} = 0\text{V}$ at IN_x	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$, See Figure 8-3 (Note 1)	150	200		$\text{kV}/\mu\text{s}$
C_I	Input capacitance (Note 2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC} = 5\text{ V}$		2		pF

7.6.2 Electrical Characteristics ($V_{CCA} = V_{CCB} = 3.3\text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 3.3\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$I_{OH} = -2\text{ mA}$ (Note 1)	$V_{CCO} - 0.4$	3.2		V
V_{OL}	Output low voltage	$I_{OL} = 2\text{ mA}$		0.1	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	$V_{IH} = V_{CCA}$ at IN_x			20	μA
I_{IL}	Low-level input leakage current	$V_{IL} = 0\text{V}$ at IN_x	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200\text{ V}$, See Figure 8-3 (Note 1)	150	200		$\text{kV}/\mu\text{s}$
C_I	Input capacitance (Note 2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1\text{ MHz}$, $V_{CC} = 3.3\text{ V}$		2		pF

7.6.3 Electrical Characteristics ($V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$)

$V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	$I_{OH} = -1 \text{ mA}$ (Note 1)	$V_{CCO} - 0.4$	2.45		V
V_{OL}	Output low voltage	$I_{OL} = 1 \text{ mA}$		0.05	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	$V_{IH} = V_{CCA}$ at IN_x			20	μA
I_{IL}	Low-level input leakage current	$V_{IL} = 0\text{V}$ at IN_x	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	$V_I = V_{CCI}$ or 0 V , $V_{CM} = 1200 \text{ V}$, See Figure 8-3 (Note 1)	150	200		$\text{kV}/\mu\text{s}$
C_I	Input capacitance (Note 2)	$V_I = V_{CC}/2 + 0.4 \times \sin(2\pi ft)$, $f = 1 \text{ MHz}$, $V_{CC} = 2.5 \text{ V}$		2		pF

Note 1: V_{CCI} = Input-side supply V_{CC} , V_{CCO} = Output-side supply V_{CC} .

Note 2: Measured from pin to Ground.

7.7 Supply Current Characteristics (Note 1)

7.7.1 Supply Current Characteristics ($V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7760						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7760L);		2.9	5.4	mA
I _{CCB}		V _{IN} = V _{CCA} (UMISO7760H)		6.8	10.6	
I _{CCA}		V _{IN} = V _{CCA} (UMISO7760L);		16.6	22.1	
I _{CCB}		V _{IN} = 0V (UMISO7760H)		6.9	10.5	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C _L = 15 pF for each channel.	1Mbps	9.6	13.3	
I _{CCB}				7.5	12.3	
I _{CCA}			10Mbps	9.7	13.9	
I _{CCB}				11.3	17.1	
I _{CCA}			100Mbps	11.9	15.6	
I _{CCB}				57.6	70.2	
UMISO7761						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7761L);		3.7	6	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7761H)		6.1	9.6	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7761L);		15.1	20.4	
I _{CCB}		V _{IN} = 0V (UMISO7761H)		8.5	12.1	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C _L = 15 pF for each channel.	1Mbps	9.4	13.3	
I _{CCB}				7.7	12.3	
I _{CCA}			10Mbps	9.8	14	
I _{CCB}				10.8	16.8	
I _{CCA}			100Mbps	14.8	21.9	
I _{CCB}				51.4	64.2	
UMISO7762						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7762L);		4.4	7	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7762H)		5.3	9	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7762L);		13.5	18.8	
I _{CCB}		V _{IN} = 0V (UMISO7762H)		10	13.8	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C _L = 15 pF for each channel.	1Mbps	9.2	13.3	
I _{CCB}				7.9	12.3	
I _{CCA}			10Mbps	10.3	14.3	
I _{CCB}				10.7	16.7	
I _{CCA}			100Mbps	21.6	28.5	
I _{CCB}				47.9	57.3	
UMISO7763						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7763L);		5.2	9	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7763H)		5.2	9	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7763L);		12.2	18	
I _{CCB}		V _{IN} = 0V (UMISO7763H)		12.2	18	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C _L = 15 pF for each channel.	1Mbps	9	14.3	
I _{CCB}				9	14.3	
I _{CCA}			10Mbps	10.6	16.6	
I _{CCB}				10.6	16.6	
I _{CCA}			100Mbps	32	44.3	
I _{CCB}				32	44.3	

7.7.2 Supply Current Characteristics ($V_{CCA} = V_{CCB} = 3.3 \text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 3.3 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7760						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7760L);		2.8	5.4	mA
I _{CCB}		V _{IN} = V _{CCA} (UMISO7760H)		6.5	10.5	
I _{CCA}		V _{IN} = V _{CCA} (UMISO7760L);		16.5	22	
I _{CCB}		V _{IN} = 0V (UMISO7760H)		6.7	10.4	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C _L = 15 pF for each channel.	1Mbps	9.5	13.2	
I _{CCB}				7	12.2	
I _{CCA}			10Mbps	9.5	13.7	
I _{CCB}				9.6	14.7	
I _{CCA}			100Mbps	11.4	15	
I _{CCB}				39.5	50.9	
UMISO7761						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7761L);		3.6	5.9	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7761H)		5.9	9.5	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7761L);		15	20.2	
I _{CCB}		V _{IN} = 0V (UMISO7761H)		8.3	11.9	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C _L = 15 pF for each channel.	1Mbps	9.4	13.2	
I _{CCB}				7.4	12.2	
I _{CCA}			10Mbps	9.6	13.7	
I _{CCB}				9.5	14.7	
I _{CCA}			100Mbps	13	20.6	
I _{CCB}				35.5	47.9	
UMISO7762						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7762L);		4.2	6.9	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7762H)		5.1	9	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7762L);		13.4	18.7	
I _{CCB}		V _{IN} = 0V (UMISO7762H)		9.8	13.7	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C _L = 15 pF for each channel.	1Mbps	9	13.2	
I _{CCB}				7.5	12.2	
I _{CCA}			10Mbps	9.7	13.7	
I _{CCB}				9.4	14.7	
I _{CCA}			100Mbps	17.4	23.6	
I _{CCB}				33.5	42.3	
UMISO7763						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7763L);		5	9	mA
I _{CCB}		V _{IN} = V _{CCI} (UMISO7763H)		5	9	
I _{CCA}		V _{IN} = V _{CCI} (UMISO7763L);		12	17.9	
I _{CCB}		V _{IN} = 0V (UMISO7763H)		12	17.9	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C _L = 15 pF for each channel.	1Mbps	8.7	14	
I _{CCB}				8.7	14	
I _{CCA}			10Mbps	9.8	15.9	
I _{CCB}				9.8	15.9	
I _{CCA}			100Mbps	24	33.7	
I _{CCB}				24	33.7	

7.7.3 Supply Current Characteristics ($V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$)

$V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7760						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7760L); V _{IN} = V _{CCA} (UMISO7760H) V _{IN} = V _{CCA} (UMISO7760L); V _{IN} = 0V (UMISO7760H)		2.7	5.3	mA
I _{CCB}				6.5	10.4	
I _{CCA}				16.5	22	
I _{CCB}				6.6	10.3	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C _L = 15 pF for each channel.	1Mbps	9.5	13.2	
I _{CCB}				7	12.2	
I _{CCA}			10Mbps	9.5	13.7	
I _{CCB}				8.9	14.1	
I _{CCA}			100Mbps	10.9	14.9	
I _{CCB}				31.0	38.8	
UMISO7761						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7761L); V _{IN} = V _{CCI} (UMISO7761H) V _{IN} = V _{CCI} (UMISO7761L); V _{IN} = 0V (UMISO7761H)		3.6	5.9	mA
I _{CCB}				5.9	9.5	
I _{CCA}				15	20.2	
I _{CCB}				8.3	11.9	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C _L = 15 pF for each channel.	1Mbps	9.3	13.2	
I _{CCB}				7.3	12.2	
I _{CCA}			10Mbps	9.5	13.7	
I _{CCB}				8.9	14.1	
I _{CCA}			100Mbps	12.5	19	
I _{CCB}				28.2	37.7	
UMISO7762						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7762L); V _{IN} = V _{CCI} (UMISO7762H) V _{IN} = V _{CCI} (UMISO7762L); V _{IN} = 0V (UMISO7762H)		4.2	6.8	mA
I _{CCB}				5	8.9	
I _{CCA}				13.3	18.6	
I _{CCB}				9.8	13.7	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C _L = 15 pF for each channel.	1Mbps	9	13.2	
I _{CCB}				7.5	12.2	
I _{CCA}			10Mbps	9.5	13.7	
I _{CCB}				8.9	14.1	
I _{CCA}			100Mbps	15.5	20.1	
I _{CCB}				26.4	33.6	
UMISO7763						
I _{CCA}	Supply Current-DC signal	V _{IN} = 0V (UMISO7763L); V _{IN} = V _{CCI} (UMISO7763H) V _{IN} = V _{CCI} (UMISO7763L); V _{IN} = 0V (UMISO7763H)		5	8.9	mA
I _{CCB}				5	8.9	
I _{CCA}				13.3	18.6	
I _{CCB}				13.3	18.6	
I _{CCA}	Supply Current-AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C _L = 15 pF for each channel.	1Mbps	9	13.2	
I _{CCB}				9	13.2	
I _{CCA}			10Mbps	9.5	14.1	
I _{CCB}				9.5	14.1	
I _{CCA}			100Mbps	21	31.6	
I _{CCB}				21	31.6	

Note 1: V_{CCI} = Input-side supply V_{CC} .

7.8 Electrical Characteristics (Dynamic)

7.8.1 Electrical Characteristics (Dynamic) ($V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 5\text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM _{MIN}	Minimum pulse width				5	ns
t _{PLH}	Propagation delay time	see Figure 8-1	4.5	8	16	ns
t _{PHL}		see Figure 8-1	4.5	8	16	ns
PWD	Pulse width distortion, $ t_{PLH} - t_{PHL} $	see Figure 8-1			2.6	ns
t _{SK(O)}	Channel-to-Channel output skew time (Note 1)	Same-direction channels			2.6	ns
t _{SK(PP)}	Part-to-Part output skew time (Note 2)			2.2	5	ns
t _R	Output signal rise time	see Figure 8-1		1	3	ns
t _F	Output signal fall time	see Figure 8-1		1	3	ns
t _{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t _{SU}	Start-up time			12	20	μs

Note 1: t_{SK(O)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

Note 2: t_{SK(PP)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.8.2 Electrical Characteristics (Dynamic) ($V_{CCA} = V_{CCB} = 3.3 \text{ V} \pm 10\%$)

$V_{CCA} = V_{CCB} = 3.3 \text{ V} \pm 10\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM _{MIN}	Minimum pulse width				5	ns
t _{PLH}	Propagation delay time	see Figure 8-1	4.5	10.6	16	ns
t _{PHL}		see Figure 8-1	4.5	10.6	16	ns
PWD	Pulse width distortion, $ t_{PLH} - t_{PHL} $	see Figure 8-1			2.6	ns
t _{SK(O)}	Channel-to-Channel output skew time (Note 1)	Same-direction channels			2.6	ns
t _{SK(PP)}	Part-to-Part output skew time (Note 2)			2.2	5	ns
t _R	Output signal rise time	see Figure 8-1		2.4	3.5	ns
t _F	Output signal fall time	see Figure 8-1		2.3	3.5	ns
t _{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t _{SU}	Start-up time			12	20	μs

Note 1: t_{SK(O)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

Note 2: t_{SK(PP)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.8.3 Electrical Characteristics (Dynamic) ($V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$)

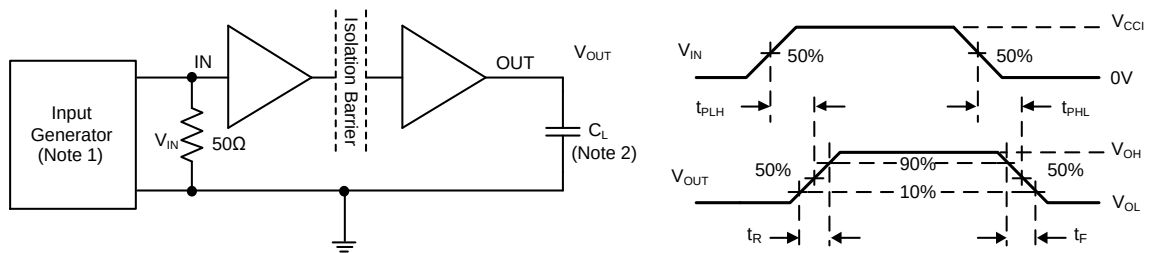
$V_{CCA} = V_{CCB} = 2.5 \text{ V} \pm 5\%$, $T_A = -40$ to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM _{MIN}	Minimum pulse width				5	ns
t _{PLH}	Propagation delay time	see Figure 8-1	5	11.8	18	ns
t _{PHL}		see Figure 8-1	5	11	18	ns
PWD	Pulse width distortion, $ t_{PLH} - t_{PHL} $	see Figure 8-1			2.6	ns
t _{SK(O)}	Channel-to-Channel output skew time (Note 1)	Same-direction channels			2.6	ns
t _{SK(PP)}	Part-to-Part output skew time (Note 2)			2.2	5	ns
t _R	Output signal rise time	see Figure 8-1		2.7	4	ns
t _F	Output signal fall time	see Figure 8-1		2.6	4	ns
t _{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t _{SU}	Start-up time			12	20	μs

Note 1: t_{SK(O)} is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.

Note 2: t_{SK(PP)} is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

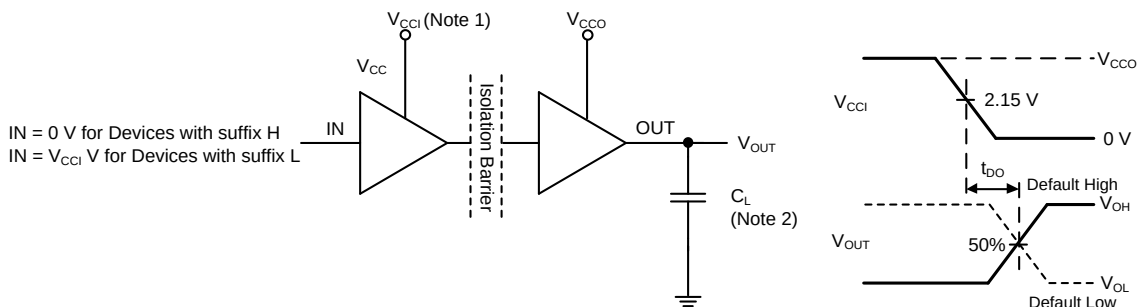
8 Parameter Measurement Information



Note 1: A square wave generator provides V_{IN} input signal with characteristics: frequency $\leq 100\text{kHz}$, 50% duty cycle, $t_R \leq 3\text{ns}$, $t_F \leq 3\text{ns}$, $Z_{OUT} = 50\Omega$. At the input, 50Ω resistor is required to terminate input generator signal. It is not needed in actual application.

Note 2: $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms

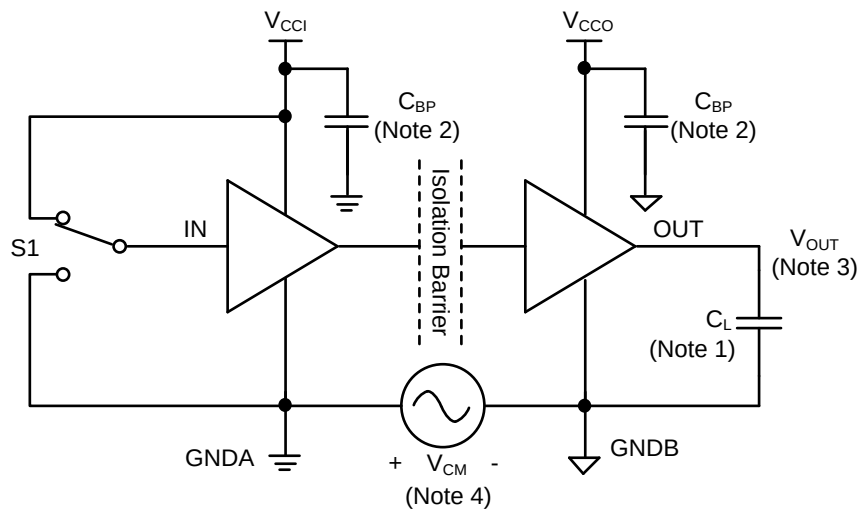


Note 1: Power Supply Ramp Rate = 10 mV/ns . V_{CCI} should ramp over 2.375V , and less than 5.5V .

Note 2: $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms

8 Parameter Measurement Information (continued)



Note 1: $C_L = 15\text{pF}$ and includes external circuit (instrumentation and fixture etc.) capacitance.

Note 2: C_{BP} ($0.1 \sim 1\mu\text{F}$) is bypass capacitance.

Note 3: Pass-fail criteria: the output must remain stable.

Note 4: The High Voltage Surge Generator generates repetitive high voltage surges with $>1\text{kV}$ amplitude, rise time $<10\text{ns}$ and fall time $<10\text{ns}$, to reach common-mode transient noise with $>150\text{kV}/\mu\text{s}$ slew rate.

Figure 8-3. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The UMISO776x devices are 6-channel digital galvanic isolators using Union's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO₂ based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovers input signal at output through a buffer stage. With this OOK architecture, the UMISO776x devices build a robust data transmission path between different power domains, without any special start-up initialization requirement.

These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and I/O buffer switching.

9.2 Functional Block Diagram

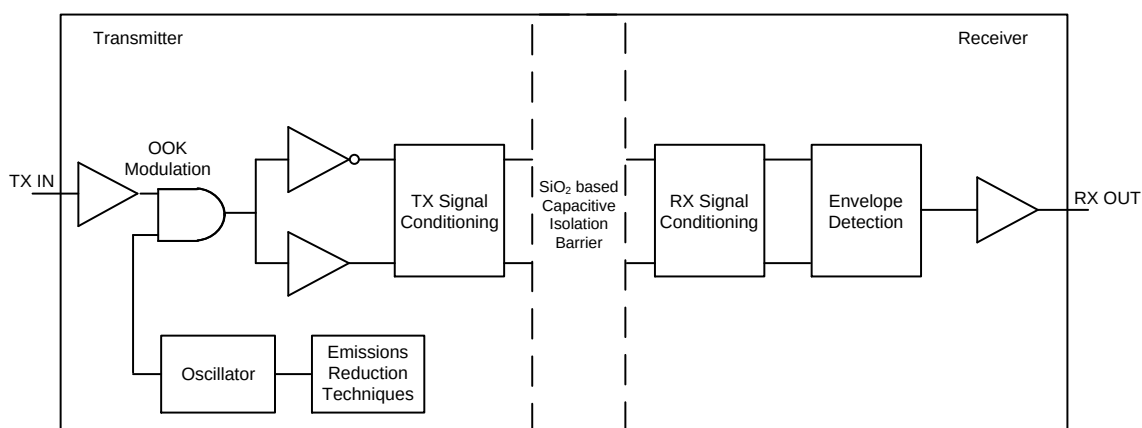


Figure 9-1. Functional Block Diagram of a Single Channel

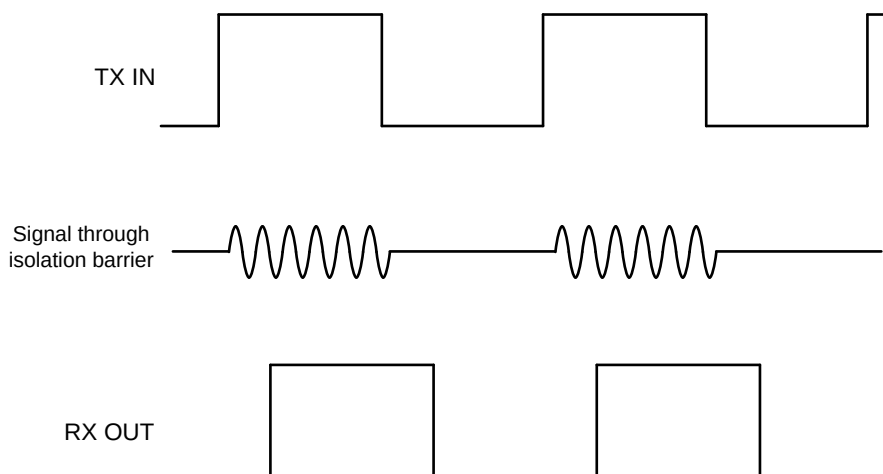


Figure 9-2. Conceptual Operation Waveforms of a Single Channel

9.3 Device Operation Modes (Note 1, 2, 3)

Table 9-1 lists the operation modes for the UMISO776x devices.

Table 9-1. Operation Mode Table (Note 1, 2, 3)

V_{CCI}	V_{CCO}	Input (IN _x)	Output (OUT _x)	Operation
X	PD	X	Undetermined	If the output side V_{CCO} is unpowered, a channel output is undetermined. (Note 4)
X	PU	X	Z	High impedance mode: A low level of Enable pin causes the output to be high impedance.
PD	PU	X	Default	Default output mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on its default option. Default is High for UMISO776xH and Low for UMISO776xL .
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input is open, the corresponding channel output goes to its default logic state. Default is High for UMISO776xH and Low for UMISO776xL .

Note 1: V_{CCI} = Input-side V_{CC} ; V_{CCO} = Output-side V_{CC} ; PU = Powered up ($V_{CC} \geq V_{CC(UVLO+)}$); PD = Powered down ($V_{CC} \leq V_{CC(UVLO-)}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.

Note 2: A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

Note 3: It is recommended to connect the enable inputs to external logic high or low level when the UMISO776x devices operate in noisy environments.

Note 4: The outputs are in undetermined state when $V_{CC(UVLO+)} < V_{CCI}$, $V_{CCO} < V_{CC(UVLO-)}$.

10 Application and Implementation

10.1 Application Information

The UMISO776x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, and eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The UMISO776x devices are the high-performance, 6-channel digital isolators. These devices come with enable pins on each side which can be used to put the respective outputs in high impedance for multi-master driving applications. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the UMISO776x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass V_{CCA} and V_{CCB} pins with $0.1\mu\text{F}$ to $1\mu\text{F}$ low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible.

10.2 Typical Application

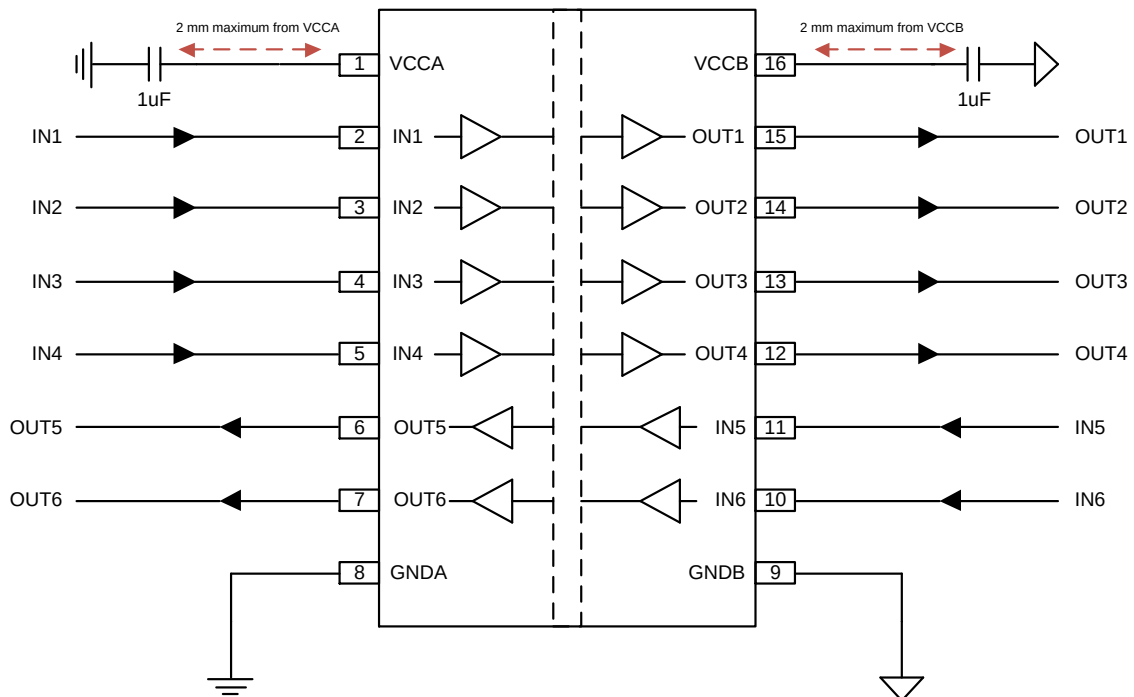
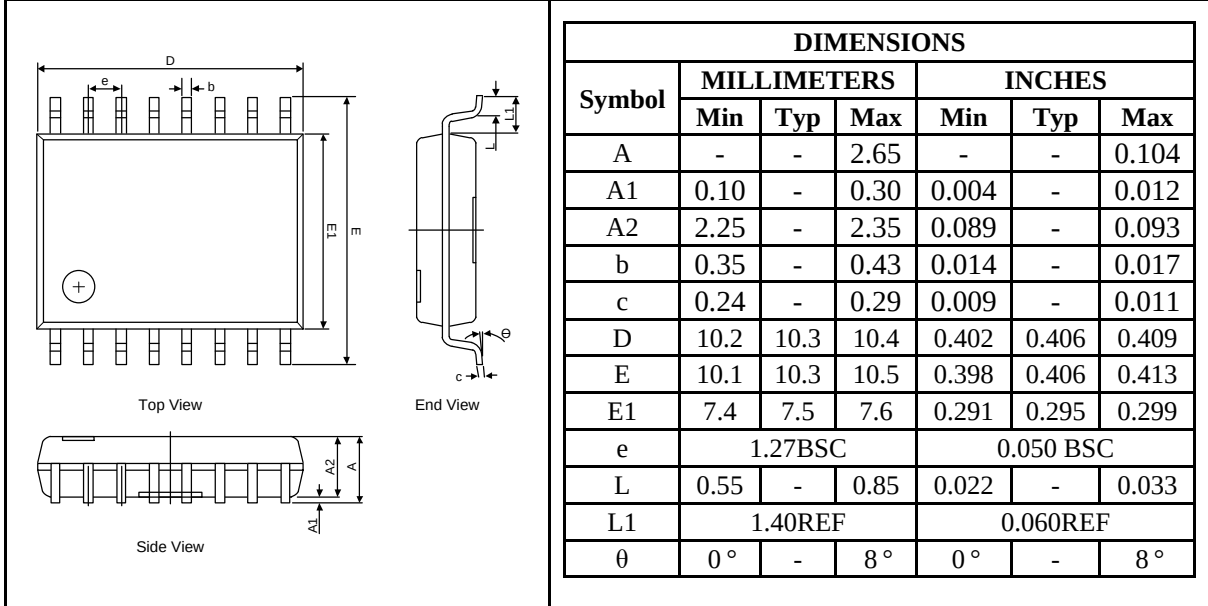


Figure 10-1. UMISO7762 Typical Application

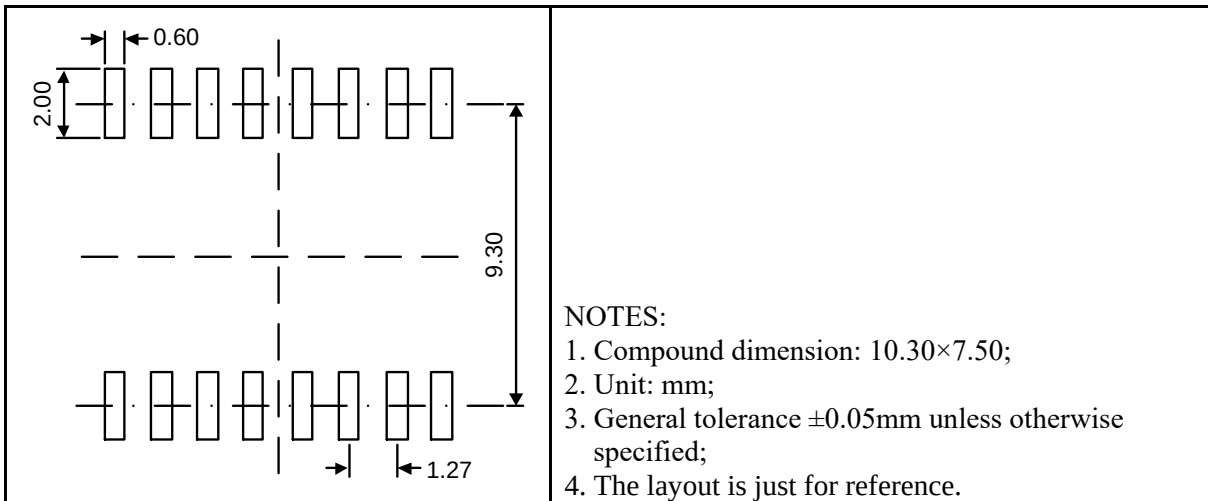
Package Information

WSOP16

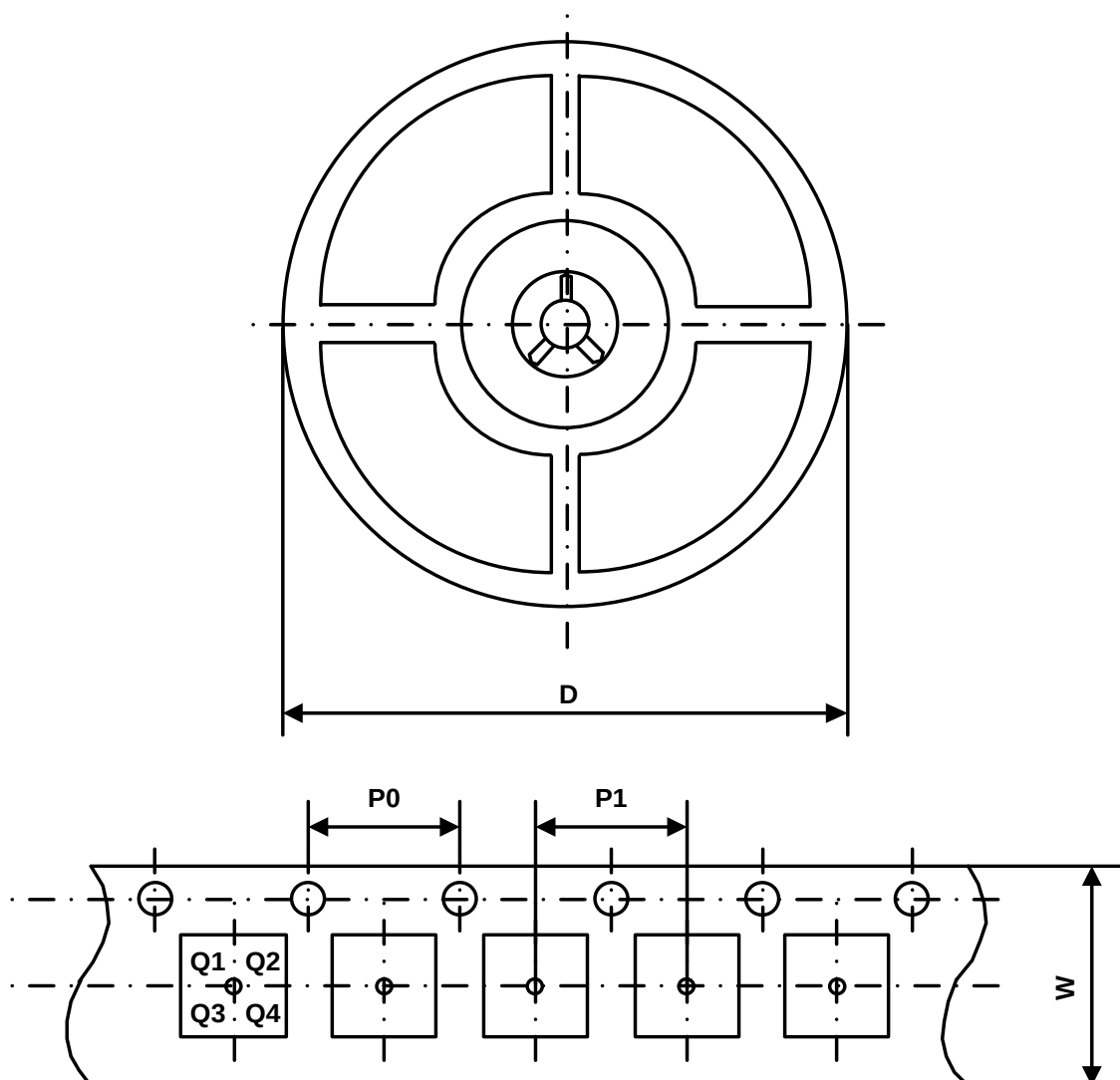
Outline Drawing



Land Pattern



Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO7760LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7760HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7761LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7761HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7762LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7762HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7763LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7763HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1

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