High-Speed Dual Channel Digital Isolators

UMISO7720 *SOP8/WSOP8/WSOP16*
UMISO7721 *SOP8/WSOP8/WSOP16*
UMISO7723 *SOP8/WSOP8/WSOP16*

1 Description

The UMISO772x series are high-performance dual-channel, unidirectional digital isolators with 3.75kV$_{RMS}$ (narrow body package) and 5kV$_{RMS}$ (wide-body package) isolation rating and DC to 150Mbps ultra-fast data rate. The devices offer high electromagnetic immunity and low emissions at low power consumption while isolating different ground domains and block high-voltage/high-current transients from sensitive or human interface circuitry. Each isolation channel has a logic input and output buffer separated by capacitive silicon dioxide (SiO_2) insulation barrier, the integrated Schmitt trigger on each input provide excellent noise immunity in automotive applications.

The UMISO7720 series feature two channels transferring signals in one direction. The UMISO7721/ UMISO7723 series have one-forward and one-reverse direction channels, making it ideal for applications such as isolated CAN, RS-485 etc. communication. The UMISO772x series features default outputs. When the input is either not powered or is open-circuit, the default output is low for devices with suffix L and high for devices with suffix H, see the Ordering Information table for suffixes associated with each option.

The UMISO772x series are available in SOP8 narrow body package, WSOP8 wide body package and WSOP16 wide body package. The devices are characterized over ambient free-air temperatures from –40 ℃ to 125 ℃.

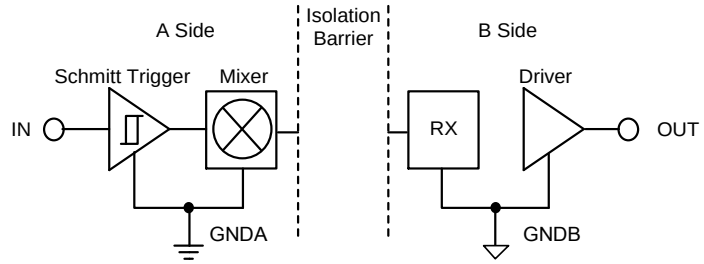
2 Features

- Data rate: DC to 150Mbps
- Robust galvanic isolation of digital signals
  - High lifetime: >40 years
  - Up to 5000 V$_{RMS}$ isolation rating (Wide body package)
  - ±200 kV/μs typical CMTI
- Wide supply range: 2.375V to 5.5V
- Extended ambient temperature range: –40 ℃ to 125 ℃
- Package options
  - SOP8 narrow body package
  - WSOP8 wide body package
  - WSOP16 wide body package
- Default output high (UMISO772xH) and low (UMISO772xL) options
- High Electromagnetic Immunity
- No start-up initialization required
- Excellent propagation delay and skew
  - Propagation delay: < 15ns
  - Pulse width distortion: < 2.6ns
- Compliant with safety regulatory
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL according to UL1577
  - IEC 61010-1 and GB 4943.1-2022

3 Applications

- Industrial Automation
- Medical Equipment
- Solar Inverter
- Motor Control
- Isolated Power Supplies
- Isolated RS-485, CAN

4 Simplified Channel Structure

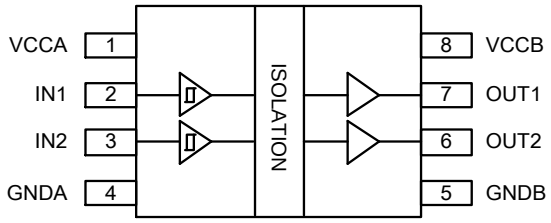


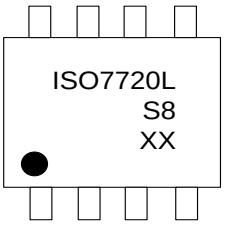
GNDA and GNDB are the isolated grounds for A side and B side respectively.

5 Ordering Information

Part Number	A Side Inputs	B Side Inputs	Default Output	Isolation Rating (V_{RMS})	Package	Shipping Qty
UMISO7720LS8	2	0	Low	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7720LWS8	2	0	Low	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7720LWSG	2	0	Low	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO7720HS8	2	0	High	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7720HWS8	2	0	High	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7720HWSG	2	0	High	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO7721LS8	1	1	Low	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7721LWS8	1	1	Low	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7721LWSG	1	1	Low	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO7721HS8	1	1	High	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7721HWS8	1	1	High	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7721HWSG	1	1	High	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO7723LS8	1	1	Low	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7723LWS8	1	1	Low	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7723LWSG	1	1	Low	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO7723HS8	1	1	High	3750	SOP8	3000pcs/13Inch Tape & Reel
UMISO7723HWS8	1	1	High	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO7723HWSG	1	1	High	5000	WSOP16	1500pcs/13Inch Tape & Reel

6 Pin Configuration and Function





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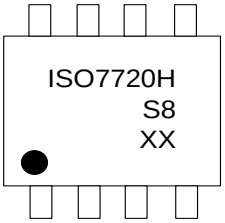
UMISO7720LS8
SOP8



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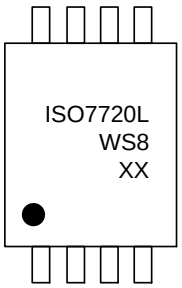

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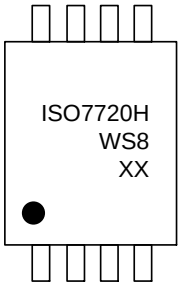

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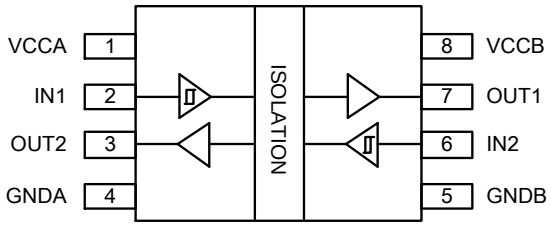
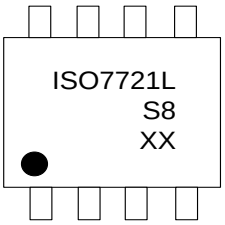
6 Pin Configuration and Function (continued)





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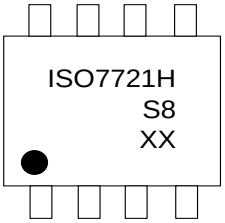

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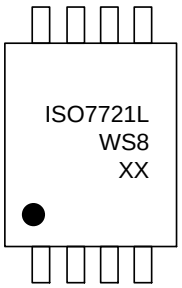

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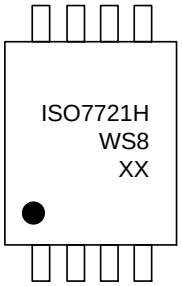

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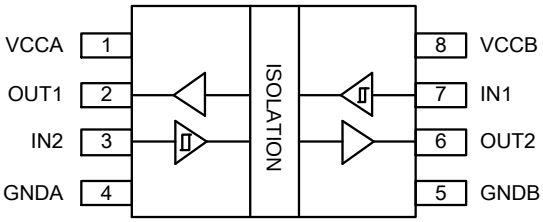
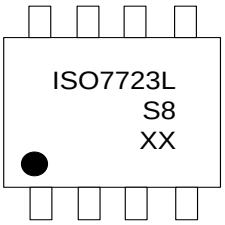
WSOP8

6 Pin Configuration and Function (continued)





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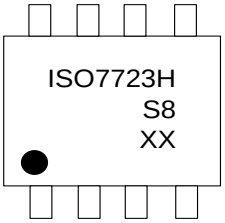

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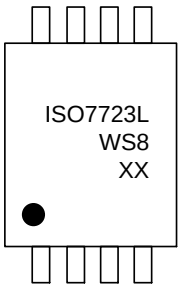

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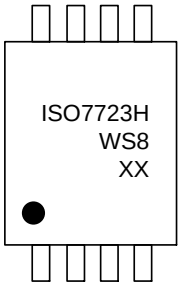


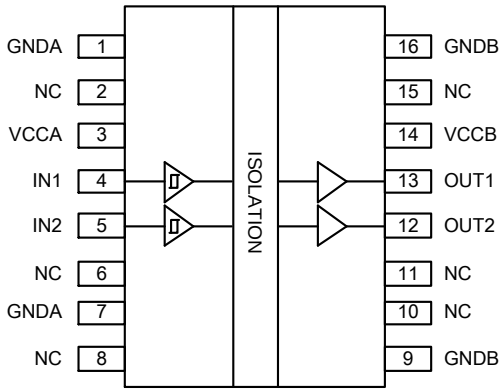
XX: Week Code
UMISO7723HWS8
WSOP8

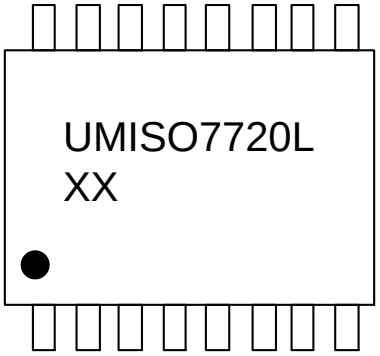
6 Pin Configuration and Function (continued)

Table 6-1. Pin functions for the UMISO772x 8-Pin SOP8 and WSOP8 packages

SOP8 and WSOP8 Pin No.			Pin Name	Function
UMISO7720	UMISO7721	UMISO7723		
1	1	1	VCCA	Power supply for isolator side A.
2	2	7	IN1	Logic input 1, corresponds to logic output 1.
3	6	3	IN2	Logic input 2, corresponds to logic output2.
4	4	4	GNDA	Ground reference for isolator side A.
5	5	5	GNDB	Ground reference for isolator side B.
7	7	2	OUT1	Logic output 1, OUT1 is the logic output for the IN1 input.
6	3	6	OUT2	Logic output 2, OUT2 is the logic output for the IN2 input.
8	8	8	VCCB	Power supply for isolator side B.

6 Pin Configuration and Function (continued)





XX: Week Code
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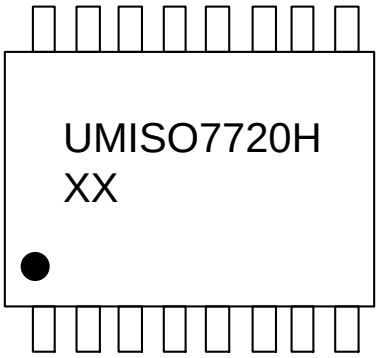

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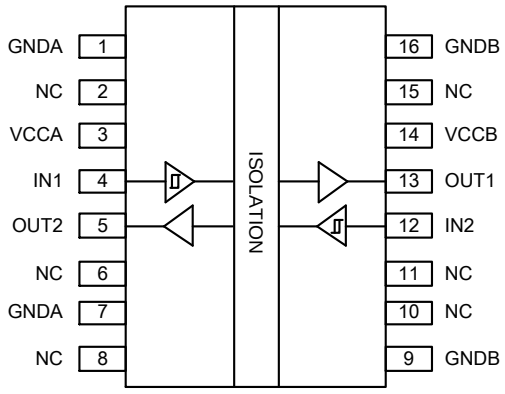
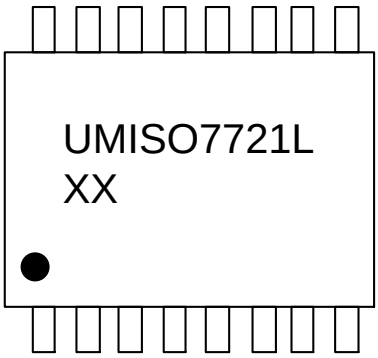
WSOP16

6 Pin Configuration and Function (continued)





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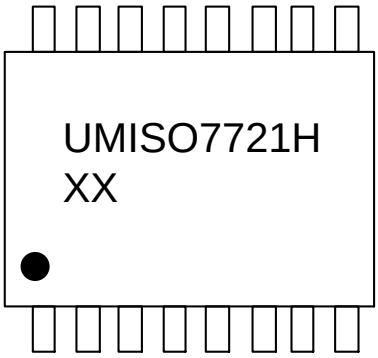
WSOP16



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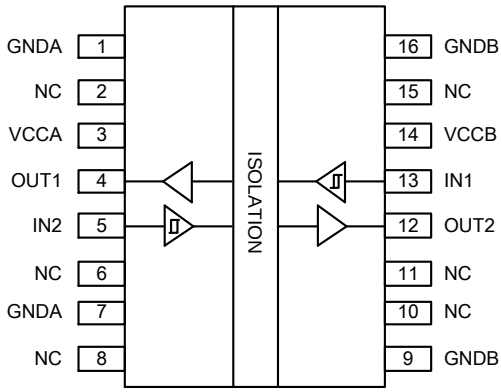
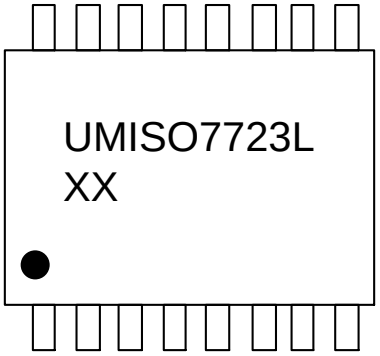
WSOP16

6 Pin Configuration and Function (continued)





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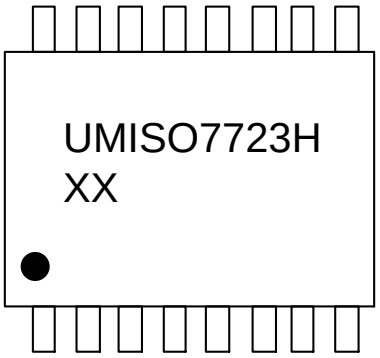


XX: Week Code
UMISO7723HWSG
WSOP16

6 Pin Configuration and Function (continued)

Table 6-2. Pin functions for the UMISO772x 16-Pin WSOP16 package

WSOP16 Pin No.			Pin Name	Function
UMISO7720	UMISO7721	UMISO7723		
1, 7	1, 7	1, 7	GNDA	Ground reference for isolator side A.
2, 6, 8	2, 6, 8	2, 6, 8	NC	Not connected. They can be left floating, tied to VCCA or tied to GNDA.
3	3	3	VCCA	Power supply for isolator side A.
4	4	13	IN1	Logic input 1, corresponds to logic output 1.
5	12	5	IN2	Logic input 2, corresponds to logic output2.
10, 11, 15	10, 11, 15	10, 11, 15	NC	Not connected. They can be left floating, tied to VCCB or tied to GNDB.
9, 16	9, 16	9, 16	GNDB	Ground reference for isolator side B.
13	13	4	OUT1	Logic output 1, OUT1 is the logic output for the IN1 input.
12	5	12	OUT2	Logic output 2, OUT2 is the logic output for the IN2 input.
14	14	14	VCCB	Power supply for isolator side B.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply voltage for isolator side A	Note 2	-0.5		6	V
V_{CCB}	Supply voltage for isolator side B	Note 2	-0.5		6	V
V_I	Voltage on INx, OUTx	Note 3	-0.5		V_{CCX} +0.5	V
V_{ESD}	Human body model (HBM),per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
I_{LU}	Latch up, per JEDEC JESD78			200		mA
I_O	Output current		-15		15	mA
T_J	Junction temperature				150	℃
T_{STG}	Storage temperature		-65		150	℃

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: All voltage values are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
Note 3: Maximum voltage must not exceed 6 V.

7.2 Recommended Operating Conditions (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CCA}	Supply voltage for isolator side A		2.375	3.3/5.0	5.5	V
V_{CCB}	Supply voltage for isolator side B		2.375	3.3/5.0	5.5	V
$V_{CC(UVLO+)}$	V_{CC} undervoltage-lockout threshold when supply voltage is rising		2	2.2	2.35	V
$V_{CC(UVLO-)}$	V_{CC} undervoltage-lockout threshold when supply voltage is falling		1.98	2.1	2.21	V
$V_{HYS(UVLO)}$	V_{CC} undervoltage-lockout threshold hysteresis		100	120	160	mV
I_{OH}	High-level output current	V_{CCO} = 5V	-4			mA
		V_{CCO} = 3.3V	-2			
		V_{CCO} = 2.5V	-1			
I_{OL}	Low-level output current	V_{CCO} = 5V			4	mA
		V_{CCO} = 3.3V			2	
		V_{CCO} = 2.5V			1	

7.2 Recommended Operating Conditions (continued)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IH}	Input High Voltage		2			V
V_{IL}	Input Low Voltage				0.8	V
DR	Data rate				150	Mbps
T_A	Ambient temperature		-40	25	125	℃

Note 1: V_{CCO} = Output-side supply V_{CC}.

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	SOP8	108	°C/W
		WSOP8	90	
		WSOP16	80	

7.4 Power Rating

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
UMISO7720						
P_D	Maximum power dissipation	V_{CCA} = V_{CCB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			176	mW
P_{DA}	Maximum power dissipation on A side				33	mW
P_{DB}	Maximum power dissipation on B side				143	mW
UMISO7721						
P_D	Maximum power dissipation	V_{CCA} = V_{CCB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			176	mW
P_{DA}	Maximum power dissipation on A side				88	mW
P_{DB}	Maximum power dissipation on B side				88	mW
UMISO7723						
P_D	Maximum power dissipation	V_{CCA} = V_{CCB} = 5.5 V, C_L = 15 pF, T_J = 150°C, Input a 75 MHz, 50% duty cycle square wave.			176	mW
P_{DA}	Maximum power dissipation on A side				88	mW
P_{DB}	Maximum power dissipation on B side				88	mW

7.5 Insulation Specifications

Symbol	Parameter	Conditions	Value		Unit
			SOP8	WSOP8/WSOP16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	4	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	4	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	16	16	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	N/A	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	N/A	I-II	
DIN V VDE V 0884-17:2021-10 (Note 1)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	450	1000	V_{RMS}
		DC voltage	637	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% product test)	5300	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC 62368-1,	5000	6000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50 μs waveform per IEC 62368-1	6500	8000	V_{PK}

7.5 Insulation Specifications (continued)

Symbol	Parameter	Conditions	Value		Unit
			SOP8	WSOP8/WSOP16	
q_{pd}	Apparent charge (Note 2)	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	pC
C_{IO}	Barrier capacitance, input to output (Note 3)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1.0	~1.0	pF
R_{IO}	Isolation resistance (Note 3)	V_{IO} = 500 V, T_A = 25 ℃	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 ℃ ≤ T_A ≤ 125 ℃	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_s = 150 ℃	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s (qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3750	5000	V_{RMS}

Note 1: This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
Note 2: The characterization charge is discharging charge (pd) caused by partial discharge.
Note 3: Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.6 Electrical Characteristics

7.6.1 Electrical Characteristics (V_{CCA} = V_{CCB} = 5 V ± 10%)

V_{CCA} = V_{CCB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	I_{OH} = -4 mA (Note 1)	V_{CCO}-0.4	4.8		V
V_{OL}	Output low voltage	I_{OL} = 4 mA		0.2	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	V_{IH} = V_{CCA} at INx			20	μA
I_{IL}	Low-level input leakage current	V_{IL} = 0V at INx	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V, See Figure 8-3 (Note 1)	150	200		kV/μs
C_I	Input capacitance (Note 2)	V_I = V_{CC} / 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 5 V		2		pF

7.6.2 Electrical Characteristics (V_{CCA} = V_{CCB} = 3.3 V ± 10%)

V_{CCA} = V_{CCB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	I_{OH} = -2 mA (Note 1)	V_{CCO}-0.4	3.2		V
V_{OL}	Output low voltage	I_{OL} = 2 mA		0.1	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	V_{IH} = V_{CCA} at INx			20	μA
I_{IL}	Low-level input leakage current	V_{IL} = 0V at INx	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V, See Figure 8-3 (Note 1)	150	200		kV/μs
C_I	Input capacitance (Note 2)	V_I = V_{CC} / 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 3.3 V		2		pF

7.6.3 Electrical Characteristics (V_{CCA} = V_{CCB} = 2.5 V ± 5%)

V_{CCA} = V_{CCB} = 2.5 V ± 5%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	Output high voltage	I_{OH} = -1 mA (Note 1)	V_{CCO}-0.4	2.45		V
V_{OL}	Output low voltage	I_{OL} = 1 mA		0.05	0.4	V
$V_{IT+(IN)}$	Logic input high		2.0			V
$V_{IT-(IN)}$	Logic input low				0.8	V
I_{IH}	High-level input leakage current	V_{IH} = V_{CCA} at INx			20	μA
I_{IL}	Low-level input leakage current	V_{IL} = 0V at INx	-20			μA
Z_O	Output impedance			50		Ω
CMTI Immunity	Common-mode transient	V_I = V_{CCI} or 0 V, V_{CM} = 1200 V, See Figure 8-3 (Note 1)	150	200		kV/μs
C_I	Input capacitance (Note 2)	V_I = V_{CC} / 2 + 0.4×sin(2πft), f = 1 MHz, V_{CC} = 2.5 V		2		pF

Note 1: V_{CCI} = Input-side supply V_{CC}, V_{CCO} = Output-side supply V_{CC}.
Note 2: Measured from pin to Ground.

7.7 Supply Current Characteristics

7.7.1 Supply Current Characteristics (V_{CCA} = V_{CCB} = 5 V ± 10%) (Note 1)

V_{CCA} = V_{CCB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UMISO7720							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7720L); V_{IN} = V_{CCI} (UMISO7720H)			1.5	3.4	mA
I_{CCB}					3.0	5.0	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7720L); V_{IN} = 0V (UMISO7720H)			6.1	8.3	
I_{CCB}					3.0	5.0	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.7	6.7	
I_{CCB}					3.3	6.7	
I_{CCA}			10Mbps		3.7	7.1	
I_{CCB}					4.3	7.5	
I_{CCA}			100Mbps		4.1	7.2	
I_{CCB}					13.8	20.1	
UMISO7721							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7721L); V_{IN} = V_{CCI} (UMISO7721H)			2.3	4.0	mA
I_{CCB}					2.3	4.0	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7721L); V_{IN} = 0V (UMISO7721H)			4.6	6.6	
I_{CCB}					4.6	6.6	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.5	6.7	
I_{CCB}					3.5	6.7	
I_{CCA}			10Mbps		3.8	7.2	
I_{CCB}					3.8	7.2	
I_{CCA}			100Mbps		7.0	13.5	
I_{CCB}					7.6	14.1	
UMISO7723							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7723L); V_{IN} = V_{CCI} (UMISO7723H)			2.2	4.3	mA
I_{CCB}					2.2	4.3	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7723L); V_{IN} = 0V (UMISO7723H)			4.5	6.6	
I_{CCB}					4.5	6.6	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.6	6.7	
I_{CCB}					3.6	6.7	
I_{CCA}			10Mbps		3.9	7.2	
I_{CCB}					3.9	7.2	
I_{CCA}			100Mbps		6.8	13.5	
I_{CCB}					7.1	14.1	

Note 1: V_{CCI} = Input-side supply V_{CC}

7.7.2 Supply Current Characteristics (V_{CCA} = V_{CCB} = 3.3 V ± 10%) (Note 1)

V_{CCA} = V_{CCB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UMISO7720							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7720L); V_{IN} = V_{CCI} (UMISO7720H)			1.4	3.4	mA
I_{CCB}					2.8	4.9	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7720L); V_{IN} = 0V (UMISO7720H)			6.0	8.2	
I_{CCB}					2.9	4.9	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C_L = 15 pF for each channel.	1Mbps		3.6	6.6	
I_{CCB}					3.1	6.6	
I_{CCA}			10Mbps		3.6	7.1	
I_{CCB}					3.8	7.1	
I_{CCA}			100Mbps		4.1	7.2	
I_{CCB}					10.1	15.8	
UMISO7721							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7721L); V_{IN} = V_{CCI} (UMISO7721H)			2.2	3.9	mA
I_{CCB}					2.2	3.9	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7721L); V_{IN} = 0V (UMISO7721H)			4.5	6.4	
I_{CCB}					4.5	6.4	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C_L = 15 pF for each channel.	1Mbps		3.5	6.6	
I_{CCB}					3.5	6.6	
I_{CCA}			10Mbps		3.7	7.1	
I_{CCB}					3.7	7.1	
I_{CCA}			100Mbps		5.7	12.8	
I_{CCB}					6.1	12.8	
UMISO7723							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7723L); V_{IN} = V_{CCI} (UMISO7723H)			2.1	4.0	mA
I_{CCB}					2.1	4.0	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7723L); V_{IN} = 0V (UMISO7723H)			4.5	6.4	
I_{CCB}					4.5	6.4	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 3.3V amplitude; C_L = 15 pF for each channel.	1Mbps		3.5	6.6	
I_{CCB}					3.5	6.6	
I_{CCA}			10Mbps		3.7	7.1	
I_{CCB}					3.7	7.1	
I_{CCA}			100Mbps		5.7	12.8	
I_{CCB}					6.1	12.8	

Note 1: V_{CCI} = Input-side supply V_{CC}

7.7.3 Supply Current Characteristics (V_{CCA} = V_{CCB} = 2.5 V ± 5%) (Note 1)

V_{CCA} = V_{CCB} = 2.5 V ± 5%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
UMISO7720							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7720L); V_{IN} = V_{CCI} (UMISO7720H)			1.3	3.3	mA
I_{CCB}					2.8	4.8	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7720L); V_{IN} = 0V (UMISO7720H)			6.0	8.2	
I_{CCB}					2.8	4.8	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.6	6.6	
I_{CCB}					3.1	6.6	
I_{CCA}			10Mbps		3.6	7.1	
I_{CCB}					3.6	7.1	
I_{CCA}			100Mbps		3.8	7.1	
I_{CCB}					8.4	12.3	
UMISO7721							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7721L); V_{IN} = V_{CCI} (UMISO7721H)			2.2	3.9	mA
I_{CCB}					2.2	3.9	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7721L); V_{IN} = 0V (UMISO7721H)			4.5	6.4	
I_{CCB}					4.5	6.4	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.4	6.6	
I_{CCB}					3.4	6.6	
I_{CCA}			10Mbps		3.6	7.1	
I_{CCB}					3.6	7.1	
I_{CCA}			100Mbps		5.4	11.2	
I_{CCB}					5.6	11.2	
UMISO7723							
I_{CCA}	Supply Current - DC signal	V_{IN} = 0V (UMISO7723L); V_{IN} = V_{CCI} (UMISO7723H)			2.1	4.0	mA
I_{CCB}					2.1	4.0	
I_{CCA}		V_{IN} = V_{CCI} (UMISO7723L); V_{IN} = 0V (UMISO7723H)			4.5	6.4	
I_{CCB}					4.5	6.4	
I_{CCA}	Supply Current - AC signal	All channels switching with 50% duty cycle square wave clock input with 2.5V amplitude; C_L = 15 pF for each channel.	1Mbps		3.5	6.6	
I_{CCB}					3.5	6.6	
I_{CCA}			10Mbps		3.6	7.1	
I_{CCB}					3.6	7.1	
I_{CCA}			100Mbps		5.4	11.2	
I_{CCB}					5.6	11.2	

Note 1: V_{CCI} = Input-side supply V_{CC}

7.8 Electrical Characteristics (Dynamic)

7.8.1 Electrical Characteristics (Dynamic) (V_{CCA} = V_{CCB} = 5 V ± 10%)

V_{CCA} = V_{CCB} = 5 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM_{MIN}	Minimum pulse width				5	ns
t_{PLH}	Propagation delay time	see Figure 8-1	4.5	8	16	ns
t_{PHL}		see Figure 8-1	4.5	8	16	ns
PWD	Pulse width distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	see Figure 8-1			2.6	ns
$t_{SK(O)}$	Channel-to-Channel output skew time (Note 1)	Same-direction			2.6	ns
$t_{SK(PP)}$	Part-to-Part output skew time (Note 2)			2.2	5	ns
t_R	Output signal rise time	see Figure 8-1		1	3	ns
t_F	Output signal fall time	see Figure 8-1		1	3	ns
t_{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t_{SU}	Start-up time			12	20	μs

Note 1: $t_{SK(O)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
Note 2: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

7.8.2 Electrical Characteristics (Dynamic) (V_{CCA} = V_{CCB} = 3.3 V ± 10%)

V_{CCA} = V_{CCB} = 3.3 V ± 10%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM_{MIN}	Minimum pulse width				5	ns
t_{PLH}	Propagation delay time	see Figure 8-1	4.5	8	16	ns
t_{PHL}		see Figure 8-1	4.5	8	16	ns
PWD	Pulse width distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	see Figure 8-1			2.6	ns
$t_{SK(O)}$	Channel-to-Channel output skew time (Note 1)	Same-direction channels			2.6	ns
$t_{SK(PP)}$	Part-to-Part output skew time (Note 2)			2.2	5	ns
t_R	Output signal rise time	see Figure 8-1		1	3.5	ns
t_F	Output signal fall time	see Figure 8-1		1	3.5	ns
t_{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t_{SU}	Start-up time			12	20	μs

Note 1: $t_{SK(O)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
Note 2: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

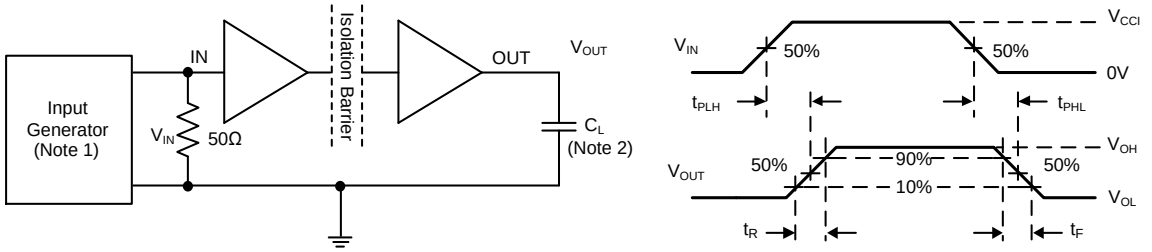
7.8.3 Electrical Characteristics (Dynamic) (V_{CCA} = V_{CCB} = 2.5 V ± 5%)

V_{CCA} = V_{CCB} = 2.5 V ± 5%, T_A = -40 to 125°C (over recommended operating conditions, unless otherwise specified).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
DR	Data rate				150	Mbps
PWM_{MIN}	Minimum pulse width				5	ns
t_{PLH}	Propagation delay time	see Figure 8-1	5	10	18	ns
t_{PHL}		see Figure 8-1	5	10	18	ns
PWD	Pulse width distortion, $\lvert t_{PLH} - t_{PHL} \rvert$	see Figure 8-1			2.6	ns
$t_{SK(O)}$	Channel-to-Channel output skew time (Note 1)	Same-direction channels			2.6	ns
$t_{SK(PP)}$	Part-to-Part output skew time (Note 2)			2.2	5	ns
t_R	Output signal rise time	see Figure 8-1		2	4	ns
t_F	Output signal fall time	see Figure 8-1		2	4	ns
t_{DO}	Default output delay time from input power loss	see Figure 8-2		60	70	μs
t_{SU}	Start-up time			12	20	μs

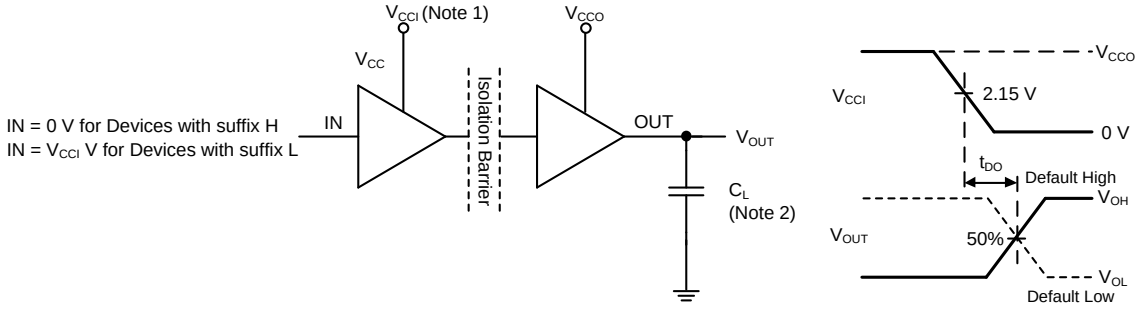
Note 1: $t_{SK(O)}$ is the skew between outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical loads.
Note 2: $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any terminals of different devices switching in the same direction while operating at identical supply voltages, temperature, input signals and loads.

8 Parameter Measurement Information



Note 1: A square wave generator provides V_{IN} input signal with characteristics: frequency≤ 100kHz, 50% duty cycle, $t_R \leq 3ns$, $t_F \leq 3ns$, $Z_{OUT} = 50\Omega$. At the input, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
Note 2: C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

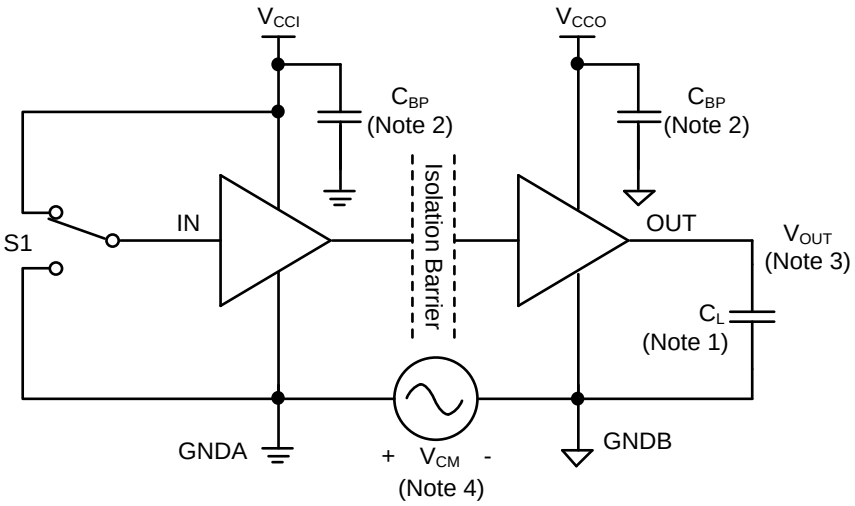
Figure 8-1. Switching Characteristics Test Circuit and Voltage Waveforms



Note 1: Power Supply Ramp Rate = 10 mV/ns. V_{CCI} should ramp over 2.375V, and less than 5.5V.
Note 2: C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance. Since the load capacitance influence the output rising time, it's a key factor in the timing characteristic measurement.

Figure 8-2. Default Output Delay Time Test Circuit and Voltage Waveforms

8 Parameter Measurement Information (continued)



Note 1: C_L = 15pF and includes external circuit (instrumentation and fixture etc.) capacitance.
Note 2: C_{BP} (0.1 ~ 1uF) is bypass capacitance.
Note 3: Pass−fail criteria: the output must remain stable.
Note 4: The High Voltage Surge Generator generates repetitive high voltage surges with >1kV amplitude, rise time <10ns and fall time <10ns, to reach common−mode transient noise with >150kV/μs slew rate.

Figure 8-3. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The UMISO772x devices are a family of automotive, 2-channel digital galvanic isolators using Union's full differential capacitive isolation technology. These devices have an ON-OFF keying (OOK) modulation scheme to transfer digital signals across the SiO_2 based isolation barrier between circuits with different power domains. The transmitter sends a high frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal and recovers input signal at output through a buffer stage. With this OOK architecture, UMISO772x devices build a robust data transmission path between different power domains, without any special start-up initialization requirement.
These devices also incorporate advanced full differential techniques to maximize the CMTI performance and minimize the radiated emissions due the high frequency carrier and I/O buffer switching.

9.2 Functional Block Diagram

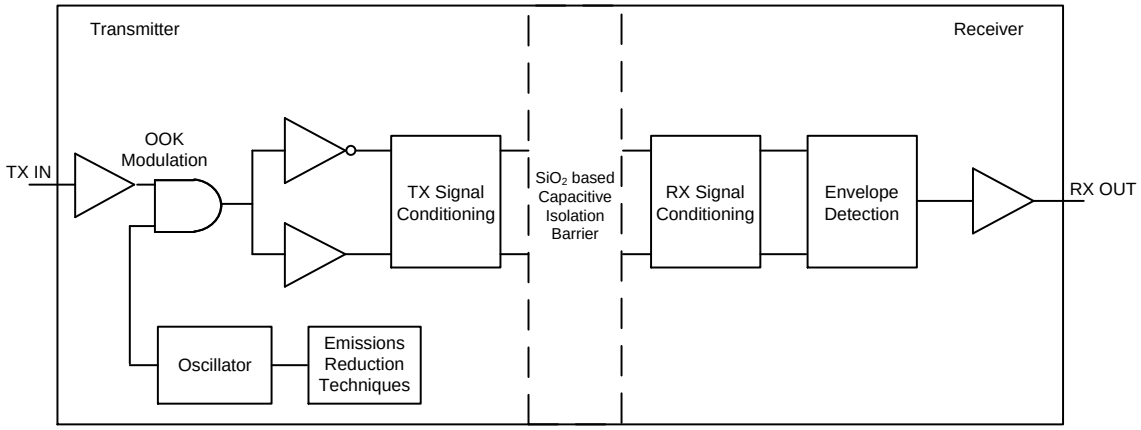


Figure 9-1. Functional Block Diagram of a Single Channel

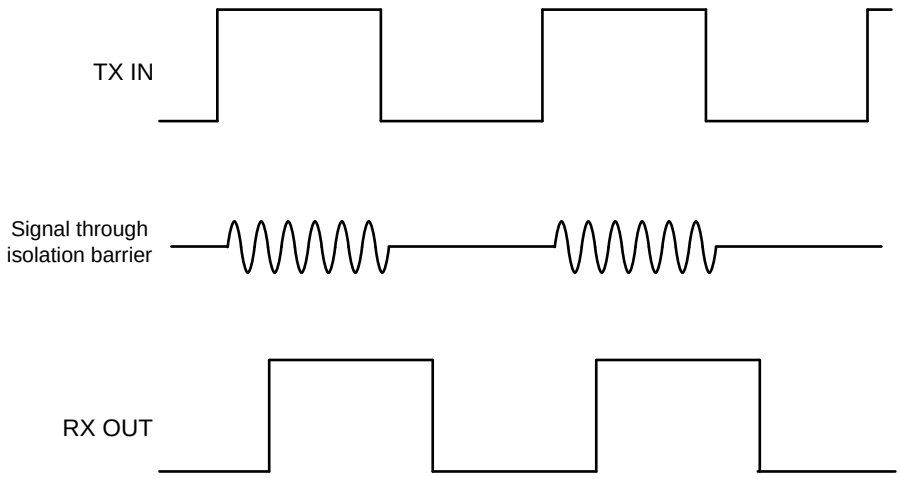


Figure 9-2. Conceptual Operation Waveforms of a Single Channel

9.3 Device Operation Modes (Note 1, 2, 3)

Table 9-1 lists the operation modes for the UMISO772x devices.

Table 9-1. Operation Mode Table (Note 1, 2)

V_{CCI}	V_{CCO}	Input (INx)	Output (OUTx)	Operation
X	PD	X	Undetermined	If the output side V_{CCO} is unpowered, a channel output is undetermined. (Note 3)
X	PU	X	Z	High impedance mode: A low level of Enable pin causes the output to be high impedance.
PD	PU	X	Default	Default output mode: When V_{CCI} is unpowered, a channel output assumes the logic state based on its default option. Default is High for UMISO772xH and Low for UMISO772xL .
PU	PU	H	H	Normal operation mode: A channel output follows the logic state of its input.
		L	L	
		Open	Default	Default output mode: When input is open, the corresponding channel output goes to its default logic state. Default is High for UMISO772xH and Low for UMISO772xL .

Note 1: V_{CCI} = Input−side V_{CC}; V_{CCO} = Output−side V_{CC}; PU = Powered up ($V_{CC} \geq V_{CC\,(UVLO+)}$); PD = Powered down ($V_{CC} \leq V_{CC\,(UVLO-)}$); X = Irrelevant; H = High level; L = Low level; Z = High Impedance.

Note 2: A strongly driven input signal can weakly power the floating V_{CC} through an internal protection diode and cause undetermined output.

Note 3: The outputs are in undetermined state when $V_{CC\,(UVLO+)} < V_{CCI}$, $V_{CCO} < V_{CC\,(UVLO-)}$.

10 Application and Implementation

10.1 Application Information

The UMISO772x isolation ICs provide complete galvanic isolation between two power domains, protecting circuits from high common-mode transients and faults, and eliminating ground loops. In many applications, digital isolators are replacing optocouplers because they can reduce the power requirements and take up less board space while offering the same isolation capability. The UMISO772x devices are the high-performance, 2-channel digital isolators. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the UMISO772x devices only require two external bypass capacitors to operate. To reduce ripple and the chance of introducing data errors, bypass V_{CCA} and V_{CCB} pins with 0.1μF to 1μF low-ESR ceramic capacitors to GNDA and GNDB respectively. Place the bypass capacitors as close to the power supply input pins as possible.

10.2 Typical Application

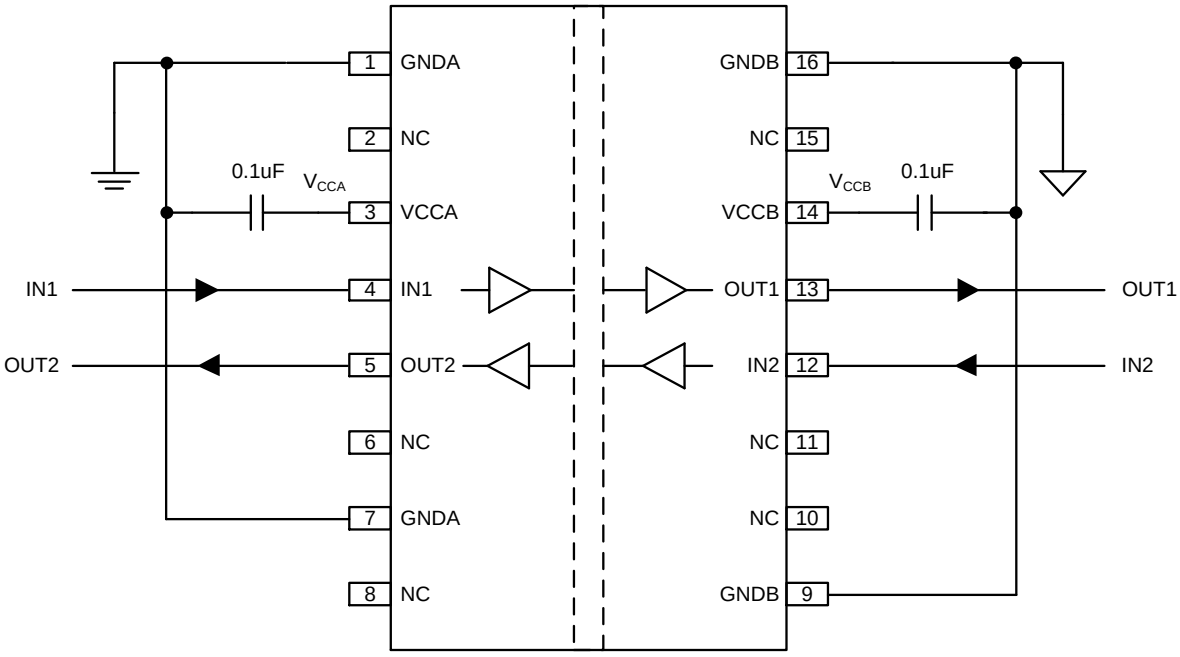
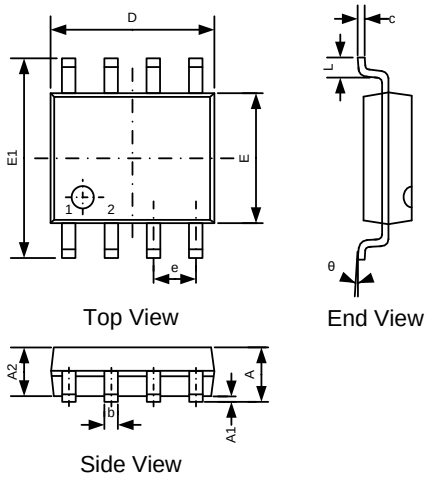


Figure 10-1. UMISO7721 Typical Application

Package Information

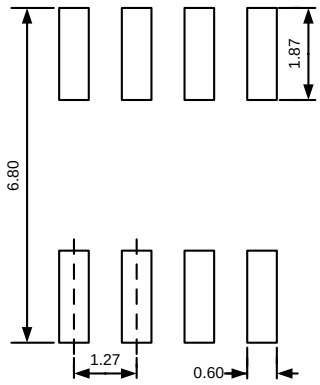
SOP8

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	-	0.25	0.004	-	0.010
A2	1.25	-	1.65	0.049	-	0.065
b	0.30	-	0.51	0.012	-	0.020
c	0.15	-	0.25	0.006	-	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.80	3.90	4.00	0.150	0.154	0.157
E1	5.80	6.00	6.20	0.228	0.236	0.244
e	1.27BSC			0.050 BSC		
L	0.40	-	1.27	0.016	-	0.050
θ	0 °	-	8 °	0 °	-	8 °

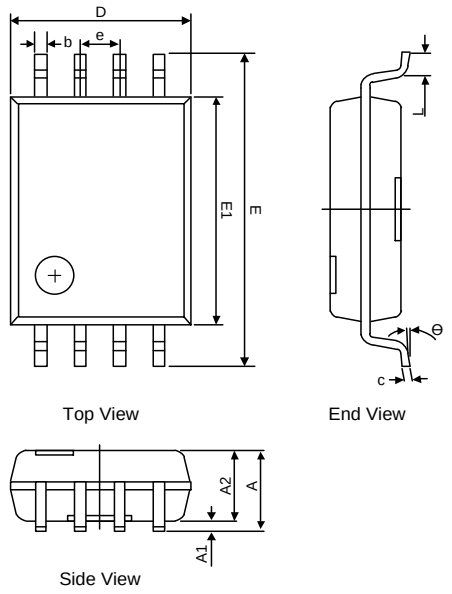
Land Pattern



NOTES:
1. Compound dimension: 4.90×3.90;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

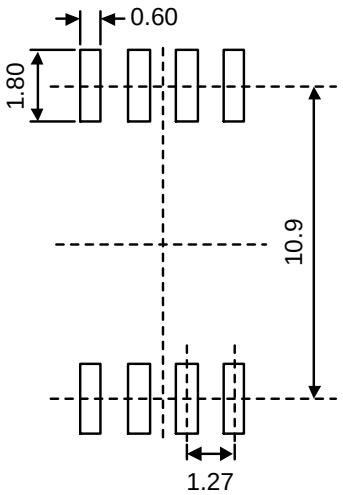
WSOP8

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.80	-	-	0.112
A1	0.36	-	0.46	0.014	-	0.018
A2	2.18	-	2.40	0.087	-	0.096
b	0.31	-	0.51	0.012	-	0.020
c	0.15	-	0.31	0.006	-	0.012
D	5.75	5.85	5.95	0.230	0.234	0.238
E	11.25	11.50	11.75	0.450	0.460	0.470
E1	7.40	7.50	7.60	0.296	0.300	0.304
e	1.27BSC			0.050 BSC		
L	0.50	-	1.00	0.020	-	0.040
θ	0 °	-	8 °	0 °	-	8 °

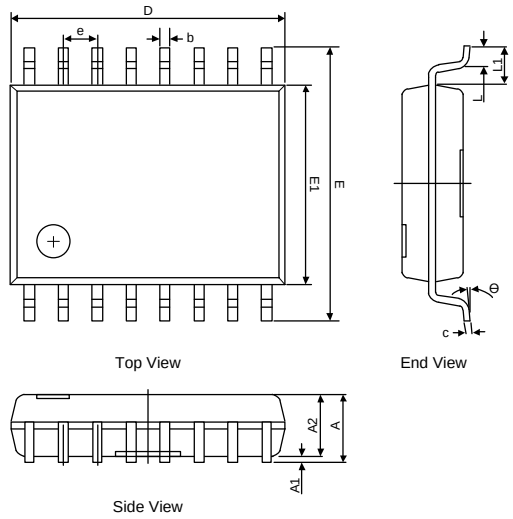
Land Pattern



NOTES:
1. Compound dimension: 5.85×7.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

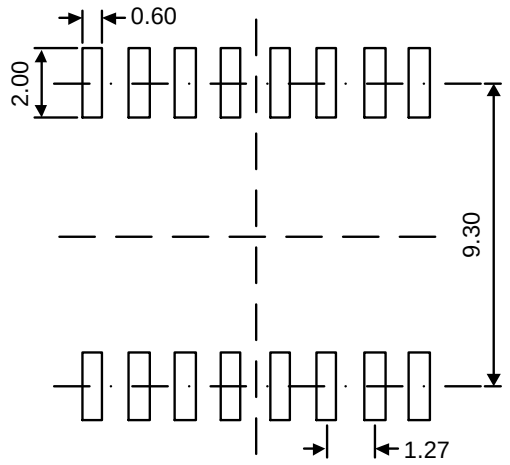
WSOP16

Outline Drawing



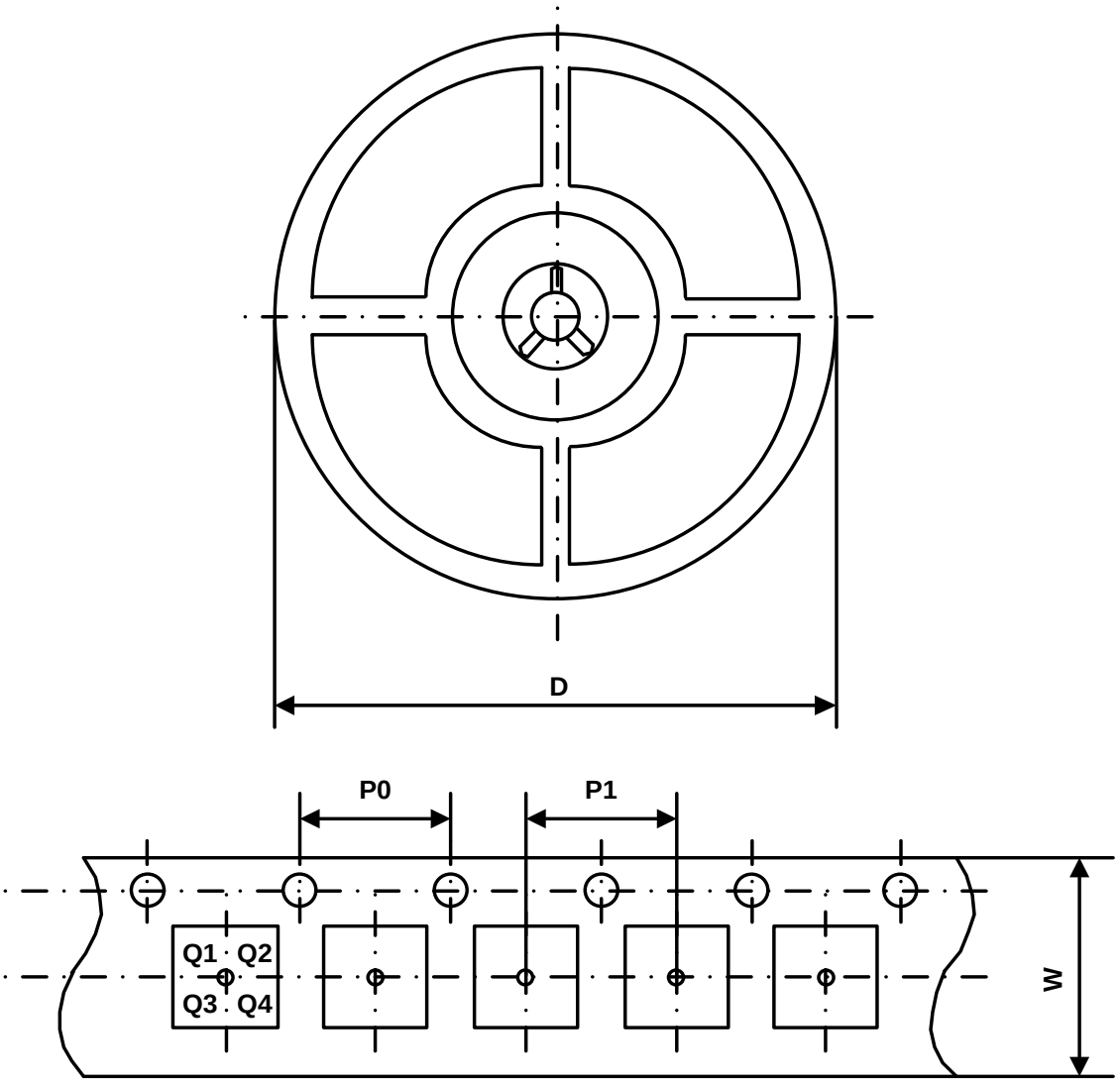
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.65	-	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	2.25	-	2.35	0.089	-	0.093
b	0.35	-	0.43	0.014	-	0.017
c	0.24	-	0.29	0.009	-	0.011
D	10.2	10.3	10.4	0.402	0.406	0.409
E	10.1	10.3	10.5	0.398	0.406	0.413
E1	7.4	7.5	7.6	0.291	0.295	0.299
e	1.27BSC			0.050 BSC		
L	0.55	-	0.85	0.022	-	0.033
L1	1.40REF			0.060REF		
θ	0°	-	8°	0°	-	8°

Land Pattern



NOTES:
1. Compound dimension: 10.30×7.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO7720LS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMISO7720HS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMISO7721LS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMISO7721HS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMISO7723LS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1
UMISO7723HS8	SOP8	12 mm	4 mm	8 mm	330 mm	Q1

Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO7720LWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7720HWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7721LWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7721HWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7723LWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7723HWS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO7720LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7720HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7721LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7721HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7723LWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO7723HWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1

GREEN COMPLIANCE

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All Union components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives. For more green compliance information, please visit:
https://www.union-ic.com/Quality.html

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