High-Speed Isolated CAN Transceiver

UMISO1050 *DUB8/WSOP8/WSOP16*
UMISO1052 *WSOP8/WSOP16*

1 Description

The UMISO105x series are an isolated CAN transceiver which is fully compatible with the ISO11898-2 standard. The devices have the logic input and output buffers separated by a silicon oxide (SiO_2) insulation barrier that provides galvanic isolation of up to 5000 V_{RMS} for UMISO105x wide body package, and up to 3750 V_{RMS} for UMISO1050 DUB8 package, which provides high electromagnetic immunity and low emissions.

The data rate of the UMISO105x series are up to 5Mbps. The devices are designed for operation in especially harsh environments that feature cross-wire, overvoltage and loss of ground protection from -40 V to 40 V, as well as -15V to 15V common-mode range. The UMISO105x series provide thermal protection and transmit data dominant time out function.

The UMISO1050 series are available in DUB8, WSOP8 wide body package and WSOP16 wide body package and The UMISO1052 series are available in WSOP8 wide body package and WSOP16 wide body package. The devices are characterized over ambient free-air temperatures from -40℃ to 125℃.

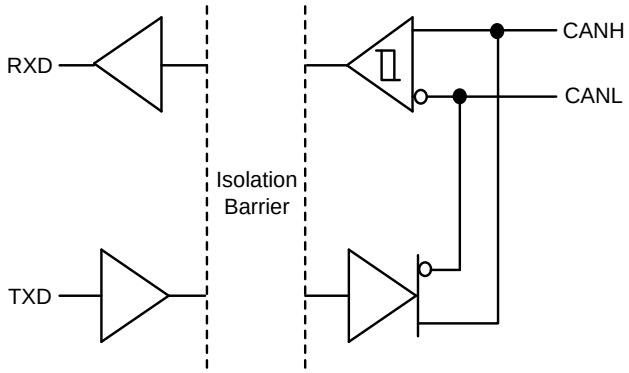
2 Features

- Fully compatible with the ISO11898-2 standard
- I/O voltage range supports 3.3 V and 5 V microprocessors
- Date rate: up to 5Mbps
- Low loop delay: 120ns (typical)
- Integrated protection increases robustness
  - Up to 5000 V_{RMS} isolation rating (Wide body packages), Up to 3750 V_{RMS} isolation rating (DUB package)
  - ±200 kV/μs typical CMTI
  - High lifetime: >40 years
  - Transmit data (TXD) dominant time out function
  - Bus fault protection of -40V to +40V
  - Over current and over temperature protection
- Compliant with safety regulatory
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL according to UL1577
  - IEC 61010-1 and GB 4943.1-2022
- Extended ambient temperature range: –40℃ to 125℃
- Available in DUB8, WSOP8 and WSOP16 packages

3 Applications

- Industrial Automation
- HVAC Automation
- Solar Inverter
- Medical Systems
- Motor Control
- Telcom

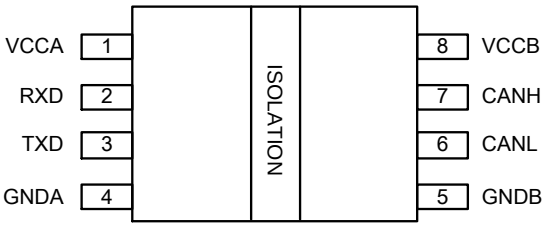
4 Simplified Channel Structure

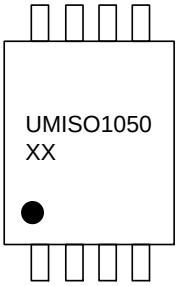


5 Ordering Information

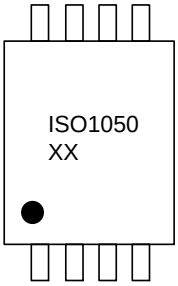
Part Number	Marking Code	Isolation Rating (V_{RMS})	Package Type	Shipping Qty
UMISO1050Z8	UMISO1050	3750	DUB8	800pcs/13Inch Tape & Reel
UMISO1050WS8	ISO1050	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO1050WSG	UMISO1050	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO1052WS8	ISO1052	5000	WSOP8	1000pcs/13Inch Tape & Reel
UMISO1052WSG	UMISO1052	5000	WSOP16	1500pcs/13Inch Tape & Reel

6 Pin Configuration and Function

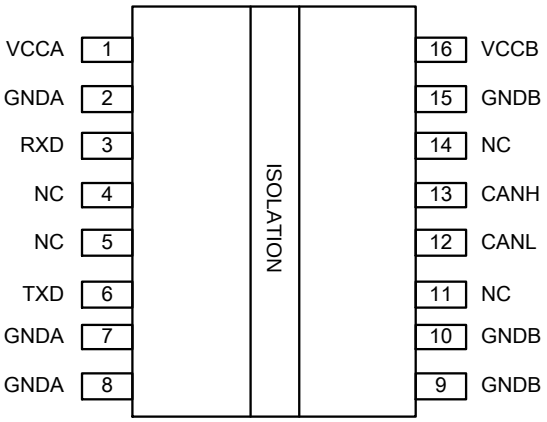


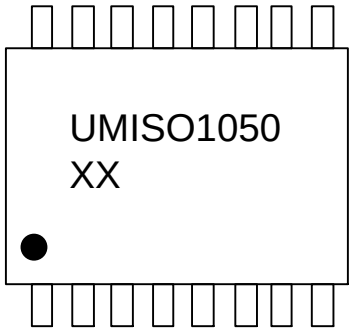


XX: Week Code
UMISO1050Z8
DUB8



XX: Week Code
UMISO1050WS8
WSOP8





XX: Week Code
UMISO1050WSG
WSOP16

6 Pin Configuration and Function (continued)

Table 6-1. Pin Functions of UMISO1050

Pin No.			Pin Name	Function
DUB8	WSOP8	WSOP16		
1	1	1	VCCA	Power supply for isolator Logic side.
4	4	2, 7, 8	GNDA	Ground reference for isolator Logic side.
2	2	3	RXD	Receive data output.
-	-	4, 5, 11, 14	NC	Not connected.
3	3	6	TXD	Transmit data input.
5	5	9, 10, 15	GNDB	Ground reference for isolator Bus side.
6	6	12	CANL	Low-level CAN bus line.
7	7	13	CANH	High-level CAN bus line.
8	8	16	VCCB	Power supply for isolator Bus side.

6 Pin Configuration and Function (continued)

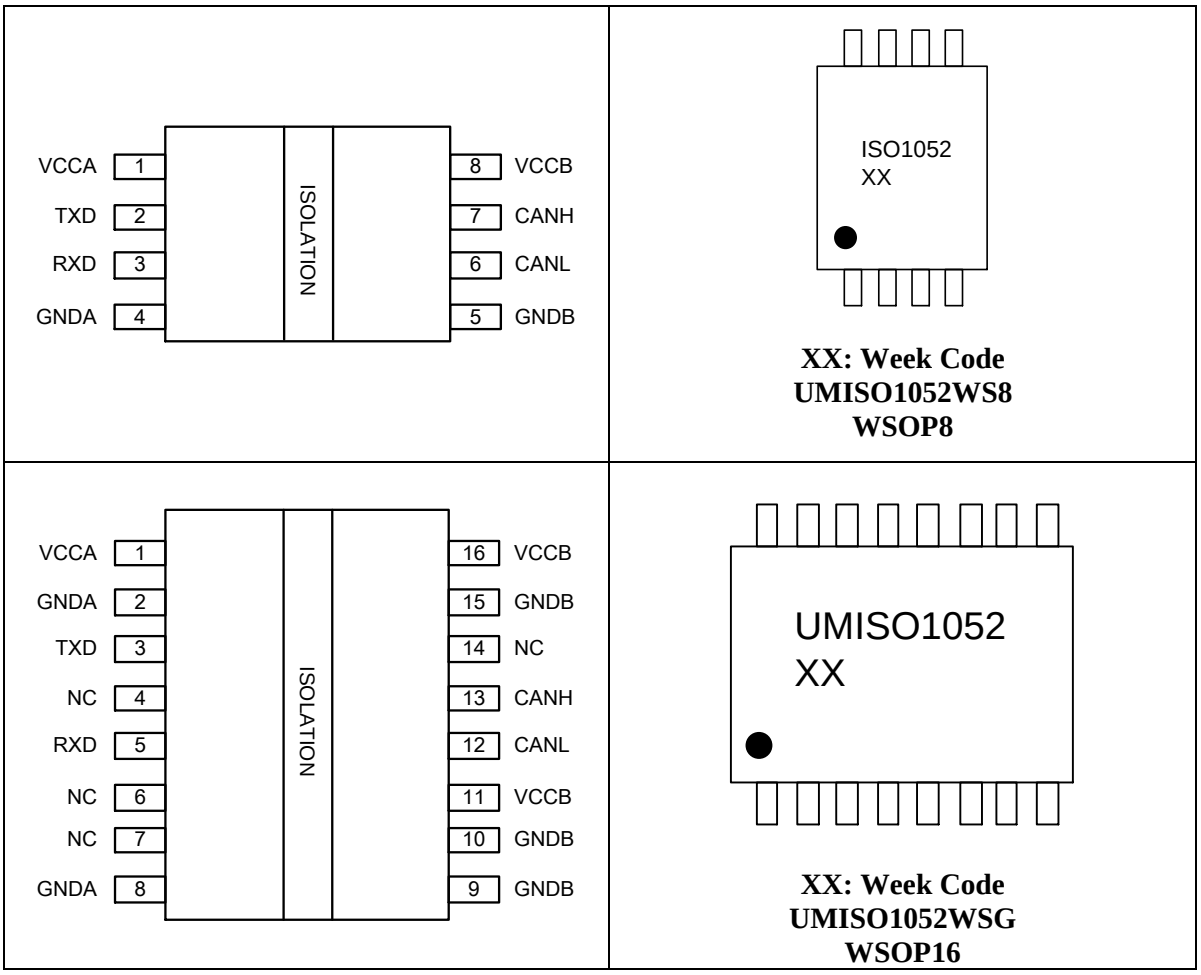


Table 6-2. Pin Functions of UMISO1052

Pin No.		Pin Name	Function
WSOP8	WSOP16		
1	1	VCCA	Power supply for isolator Logic side.
4	2, 8	GNDA	Ground reference for isolator Logic side.
3	5	RXD	Receive data output.
-	4, 6, 7, 14	NC	Not connected.
2	3	TXD	Transmit data input.
5	9, 10, 15	GNDB	Ground reference for isolator Bus side.
6	12	CANL	Low-level CAN bus line.
7	13	CANH	High-level CAN bus line.
8	11, 16	VCCB	Power supply for isolator Bus side.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter		Min	Typ	Max	Unit
V_{CCA}	Power supply for isolator Logic side		-0.5		+6	V
V_{CCB}	Power supply for isolator Bus side		-0.5		+6	V
V_{BUS}	Voltage range on CANH, CANL		-40		+40	V
V_{DIF}	Voltage range between CANH and CANL		-40		+40	V
V_I	Voltage range on TXD (Note 3)		-0.5		V_{CCA}+0.5	V
V_O	Voltage range on RXD (Note 3)		-0.5		V_{CCA}+0.5	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	All pins		±8		kV
	Contact discharge, per IEC 61000-4-2	Bus terminals to GNDB		±8		kV
I_{LU}	Latch up, per JEDEC JESD78			200		mA
T_J	Junction temperature				150	℃
T_{STG}	Storage temperature		-65		150	℃

Note 1: Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
Note 2: All voltage values, except differential I/O bus voltages, are with respect to ground terminal.
Note 3: Maximum voltage must not exceed 6 V

7.2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
V_{CCA}	Power supply for isolator Logic side	2.375		5.5	V
V_{CCB}	Power supply for isolator Bus side	4.5		5.5	V
V_{IH}	Input High Voltage	2			V
V_{IL}	Input Low Voltage			0.8	V
T_A	Ambient temperature	-40		125	℃

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	DUB8	70	°C/W
		WSOP8	105	°C/W
		WSOP16	82	°C/W

7.4 Insulation Specifications

Symbol	Parameter	Conditions	Value		Unit
			DUB8	WSOP8/WSOP16	
CLR	External clearance	Shortest terminal-to-terminal distance through air	6.1	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	6.8	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	16	16	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-III	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	N/A	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	N/A	I-II	
DIN V VDE V 0884-17:2021-10 (Note 1)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	637	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	450	1000	V_{RMS}
		DC voltage	637	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% product test)	5300	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC 62368-1,	5000	6000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50 μs waveform per IEC 62368-1	6500	8000	V_{PK}

7.4 Insulation Specifications (Continued)

Symbol	Parameter	Conditions	Value		Unit
			DUB8	WSOP8/WSOP16	
q_{pd}	Apparent charge (Note 2)	Method a, after input/output safety test of the subgroup 2/3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s; $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10 s	≤5	≤5	pC
		Method b, at routine test (100% production test) and preconditioning (type test) $V_{ini} = 1.2 \times V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1 s (method b1) or $V_{pd(m)} = V_{ini}$, $t_m = t_{ini}$ (method b2)	≤5	≤5	pC
C_{IO}	Barrier capacitance, input to output (Note 3)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	~1.0	~1.0	pF
R_{IO}	Isolation resistance (Note 3)	V_{IO} = 500 V, T_A = 25 ℃	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 ℃ ≤ T_A ≤ 125 ℃	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150 ℃	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	$V_{TEST} = V_{ISO}$, t = 60 s(qualification) $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	3750	5000	V_{RMS}

Note 1: This coupler is suitable for “safe electrical insulation” only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
Note 2: The characterization charge is discharging charge (pd) caused by partial discharge.
Note 3: Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.5 Electrical Characteristics

7.5.1 Electrical Characteristics (Static)

T_J = -40℃ to +150℃, V_{CCA} = 2.375 V to 5.5 V, V_{CCB} = 4.5 V to 5.5 V, R_L = 60Ω, C_L = 100pF (unless otherwise noted). Typical values are at V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Power supply						
I_{CCA}	Supply current logic side	V_I = V_{CCA}, V_{CCA} = 5.0 V		2.3	5	mA
I_{CCA}	Supply current logic side	V_I = 0 V, V_{CCA} = 5.0 V		4.6	8	mA
I_{CCB}	Supply current bus side	V_I = 0 V, bus dominant, R_L = 60 Ω		55	73	mA
I_{CCB}	Supply current bus side	V_I = V_{CCA}		3.9	12	mA
$V_{CCA(UVLO)RIS}$	Rising under voltage detection, V_{CCA}		2	2.2	2.35	V
$V_{CCA(UVLO)FAL}$	Falling under voltage detection, V_{CCA}		1.98	2.1	2.21	V
$V_{CCB(UVLO)RIS}$	Rising under voltage detection, V_{CCB}		3.7	4.0	4.3	V
$V_{CCB(UVLO)FAL}$	Falling under voltage detection, V_{CCB}		3.5	3.85	4.25	V
CAN transmit data input; pin TXD						
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IH}	High-level input current	TXD = V_{CCA}			10	uA
I_{IL}	Low-level input current	TXD = 0 V	-10			uA
C_I	Input capacitance			5	10	pF
CAN receive data output; pin RXD						
V_{OH}	High level output voltage with V_{CCA} = 5 V	I_{OH} = -4mA, see figure 8-6	V_{CCA} -0.8	4.8		V
		I_{OH} = -20uA, see figure 8-6	V_{CCA} -0.1	5		V
V_{OH}	High level output voltage with V_{CCA} = 3.3 V	I_{OH} = -4mA, see figure 8-6	V_{CCA} -0.8	3.1		V
		I_{OH} = -20uA, see figure 8-6	V_{CCA} -0.1	3.3		V
V_{OL}	Low level output voltage	I_{OL} = 4mA, see figure 8-6		0.2	0.4	V
		I_{OL} = 20uA, see figure 8-6		0	0.1	V

7.5.1 Electrical Characteristics (Static)---continued

T_J = -40℃ to +150℃, V_{CCA} = 2.375 V to 5.5 V, V_{CCB} = 4.5 V to 5.5 V, R_L = 60Ω, C_L = 100pF (unless otherwise noted). Typical values are at V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
$V_{O(DOM)}$	Dominant output voltage	TXD = 0 V; t < $t_{DTO(TXD)}$; R_L = 60 Ω; pin CANH, see figure 8-1 and 8-2	2.75	3.5	4.5	V
		TXD = 0 V; t < $t_{DTO(TXD)}$; R_L = 60 Ω; pin CANL, see figure 8-1 and 8-2	0.5	1.5	2.25	V
$V_{OD(DOM)}$	Dominant differential output voltage	TXD = 0V; t < $t_{DTO(TXD)}$; 50 Ω ≤ R_L ≤ 65 Ω, see figure 8-1 and 8-2	1.5		3	V
		TXD = 0V; t < $t_{DTO(TXD)}$; 45 Ω ≤ R_L ≤ 70 Ω, see figure 8-1 and 8-2	1.4		3.3	V
		TXD = 0V; t < $t_{DTO(TXD)}$; R_L = 2240 Ω, see figure 8-1 and 8-2	1.5		5	V
$V_{O(REC)}$	Recessive output voltage	TXD = V_{CCA}; R_L = 60 Ω, see figure 8-1 and 8-2	2	0.5V_{CCB}	3	V
$V_{OD(REC)}$	Recessive differential output voltage	TXD = V_{CCA}; R_L = open	-100		100	mV
		TXD = V_{CCA}; R_L = 60 Ω, see figure 8-1 and 8-2	-50		50	mV
$V_{OC(DOM)}$	Common-mode output voltage (Dominant)	See figure 8-7	2	2.5	3	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See figure 8-7		0.3		V
$I_{OS(DOM)}$	Dominant short-circuit output current	TXD = 0 V; CANH = -15 V to 40 V; CANL = open	-100	-75		mA
		TXD = 0 V; CANL = -15 V to 40 V; CANH = open		75	100	mA
$I_{OS(REC)}$	Recessive short-circuit output current	TXD = V_{CCA}; -27 V ≤ CANH = CANL ≤ 32 V	-5		5	mA

7.5.1 Electrical Characteristics (Static)---continued

T_J = -40℃ to +150℃, V_{CCA} = 2.375 V to 5.5 V, V_{CCB} = 4.5 V to 5.5 V, R_L = 60Ω, C_L = 100pF (unless otherwise noted). Typical values are at V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
V_{TH}	Differential receiver threshold voltage	-15 V ≤ CANH, CANL ≤ 15 V	0.5		0.9	V
$V_{ID(DOM)}$	Receiver dominant voltage	-15 V ≤ CANH, CANL ≤ 15 V	0.9		9	V
$V_{ID(REC)}$	Receiver recessive voltage	-15 V ≤ CANH, CANL ≤ 15 V	-4		0.5	V
V_{HYS}	Differential receiver hysteresis voltage	-15 V ≤ CANH, CANL ≤ 15 V	50		300	mV
R_I	Input resistance	TXD = V_{CCA};	15	30	40	kΩ
ΔR_I	Input resistance deviation, [1 – ($R_{IN(CANH)}$ / $R_{IN(CANL)}$)] × 100 %	TXD = V_{CCA};	-3		3	%
R_{ID}	Differential input resistance	TXD = V_{CCA};	30	60	80	kΩ
C_{IN}	Common-mode input capacitance to ground				20	pF
C_{ID}	Differential input capacitance				10	pF
CMTI	Common-mode transient immunity	V_I = V_{CCA} or 0 V, V_{CM} = 1200 V, see figure 8-12	150	200		kV/μs
Thermal Protection						
$T_{J(SD)}$	Thermal shutdown threshold	Temperature rising		185		℃

7.5.2 Electrical Characteristics (Dynamic)

T_J = -40℃ to +150℃, V_{CCA} = 2.375 V to 5.5 V, V_{CCB} = 4.5 V to 5.5 V, R_L = 60Ω, C_L = 100pF (unless otherwise noted). Typical values are at V_{CCA} = 3.3 V, V_{CCB} = 5 V, T_A = 25℃.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Device switching characteristics						
$t_{PROP(LOOP1)}$	Total loop delay, driver input TXD to receiver RXD, recessive to dominant	See figure 8-8	90	120	210	ns
$t_{PROP(LOOP2)}$	Total loop delay, driver input TXD to receiver RXD, dominant to recessive	See figure 8-8	90	120	210	ns
Driver switching characteristics						
t_{PLH}	Propagation delay time, recessive to dominant output	See figure 8-4		53	110	ns
t_{PHL}	Propagation delay time, dominant to recessive output			55	110	ns
t_R	Differential output signal rise time			28	50	ns
t_F	Differential output signal fall time			30	63	ns
$t_{DTO(TXD)}$	TXD dominant time-out time	C_L = 100pF, see figure 8-9	0.8	2.6	6.5	ms
Receiver switching characteristics						
t_{PLH}	Propagation delay time, low to high level output	See figure 8-6	66	80	130	ns
t_{PHL}	Propagation delay time, high to low level output		51	77	105	ns
t_R	Output signal rise time(RXD)			2.6	6	ns
t_F	Output signal rise time(RXD)			2	6	ns
FD timing parameters, see figure 8-11						
$t_{BIT(BUS)}$	Transmitted recessive bit width	$t_{BIT(TXD)}$ = 500ns	435		530	ns
		$t_{BIT(TXD)}$ = 200ns	155		210	ns
$t_{BIT(RXD)}$	Bit time on pin RXD	$t_{BIT(TXD)}$ = 500ns	400		550	ns
		$t_{BIT(TXD)}$ = 200ns	120		220	ns
Δt_{REC}	Receiver timing symmetry	$t_{BIT(TXD)}$ = 500ns	-65		40	ns
		$t_{BIT(TXD)}$ = 200ns	-45		15	ns

8 Parameter Measurement Information

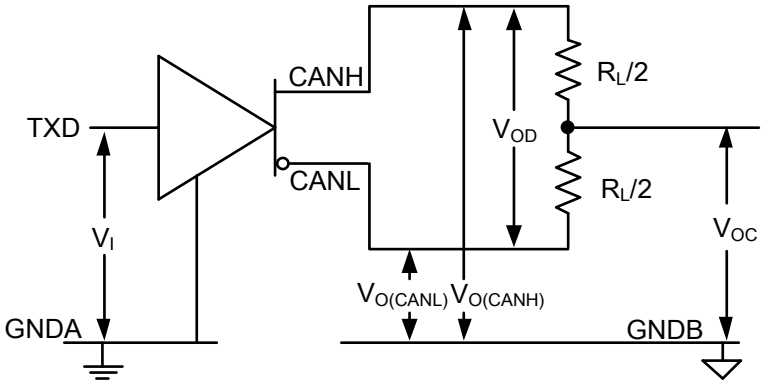


Figure 8-1. Driver Voltage, Current and Test Definitions

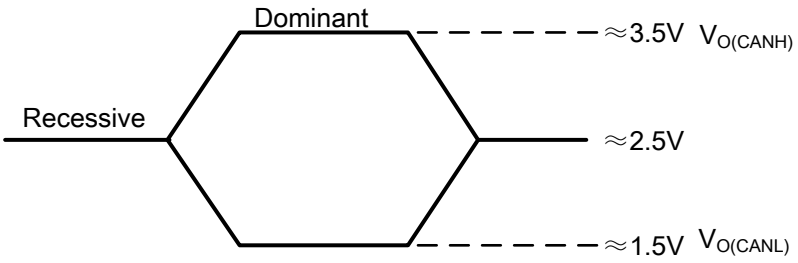


Figure 8-2. Bus Logic State Voltage Definitions

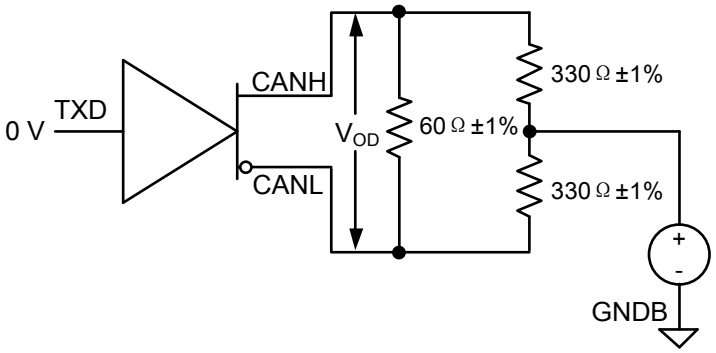
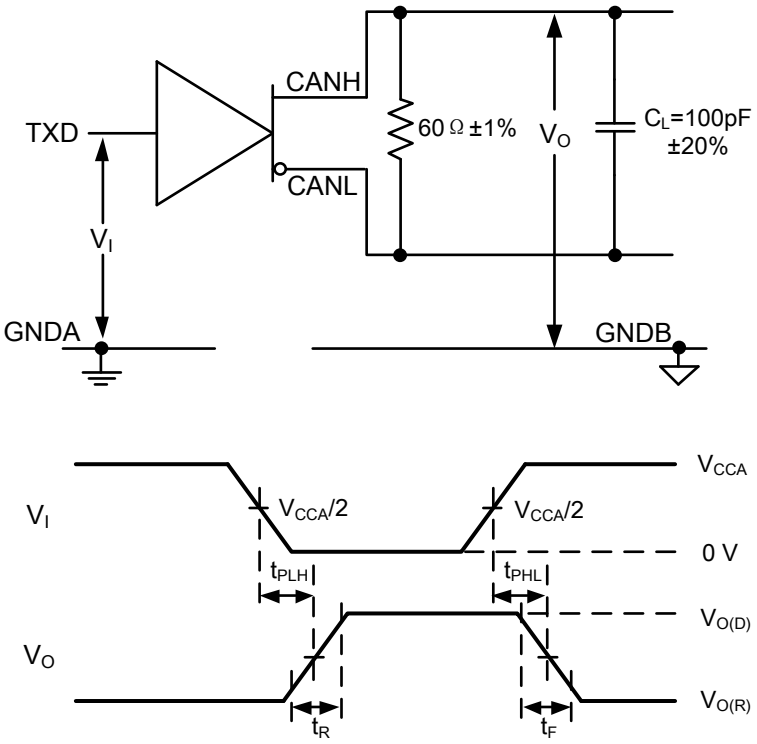


Figure 8-3. Driver V_{OD} With Common-Mode Loading Test Circuit

8 Parameter Measurement Information (continued)



Note 1: The input pulse is supplied by a generator having the following characteristics: PRR≤125 kHz, 50% duty cycle, t_R≤6 ns, t_F≤6 ns, Z_O = 50 Ω.
Note 2: C_L includes instrumentation and fixture capacitance within ±20%.

Figure 8-4. Driver Test Circuit and Voltage Waveforms

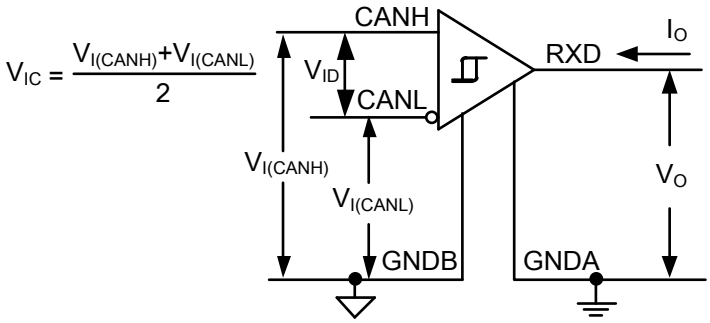
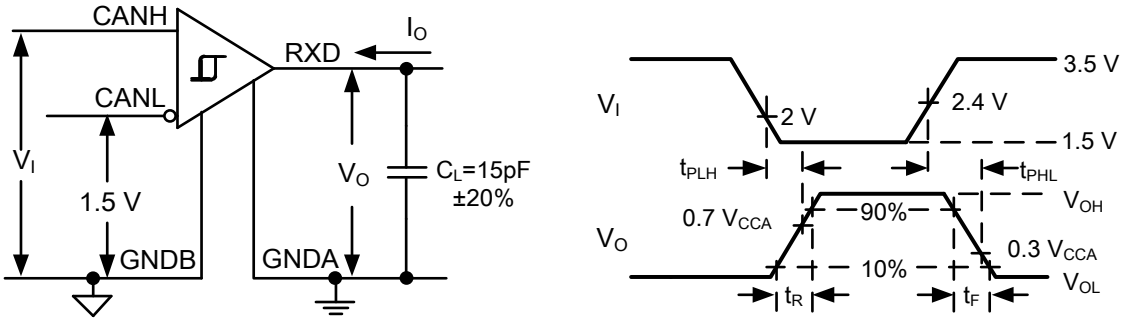


Figure 8-5. Receiver Voltage and Current Definitions

8 Parameter Measurement Information (continued)



Note 1: The input pulse is supplied by a generator having the following characteristics: PRR≤125 kHz, 50% duty cycle, t_R≤6 ns, t_F≤6 ns, Z_O = 50 Ω.
Note 2: C_L includes instrumentation and fixture capacitance within ±20%.

Figure 8-6. Receiver Test Circuit and Voltage Waveforms

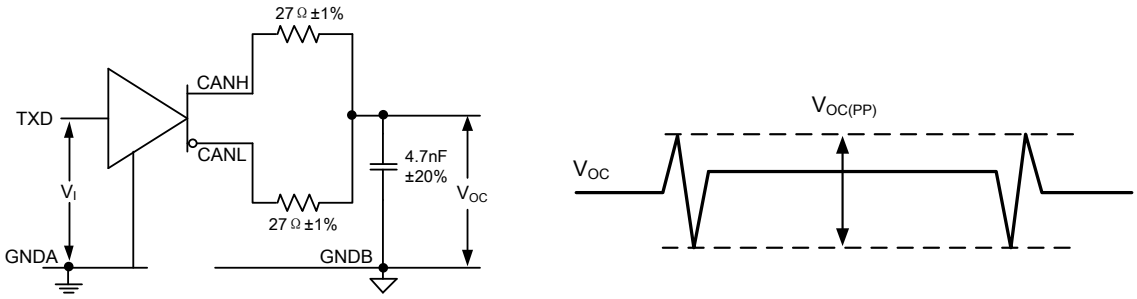


Figure 8-7. Peak-to-Peak Output Voltage Test Circuit and Waveform

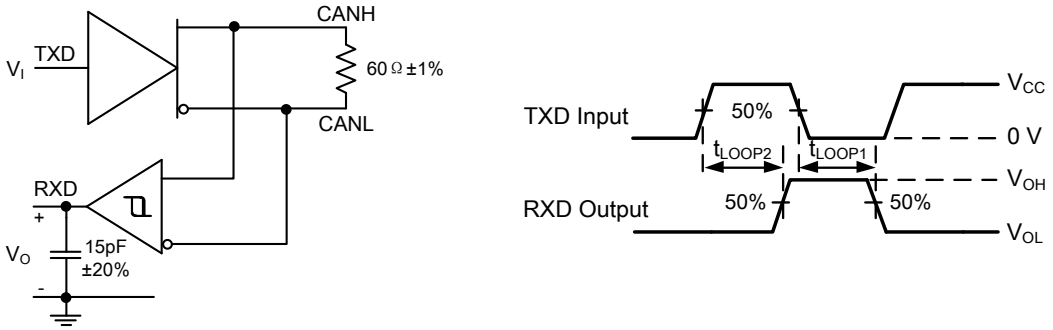


Figure 8-8. t_{LOOP} Test Circuit and Voltage Waveforms

8 Parameter Measurement Information (continued)

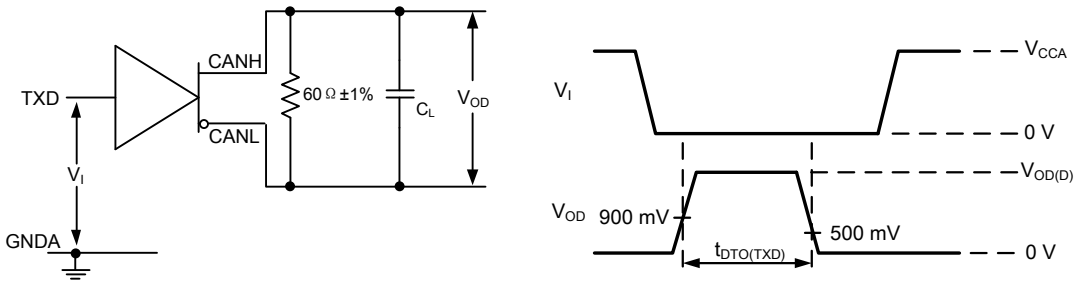


Figure 8-9. Dominant Time-out Test Circuit and Voltage Waveforms

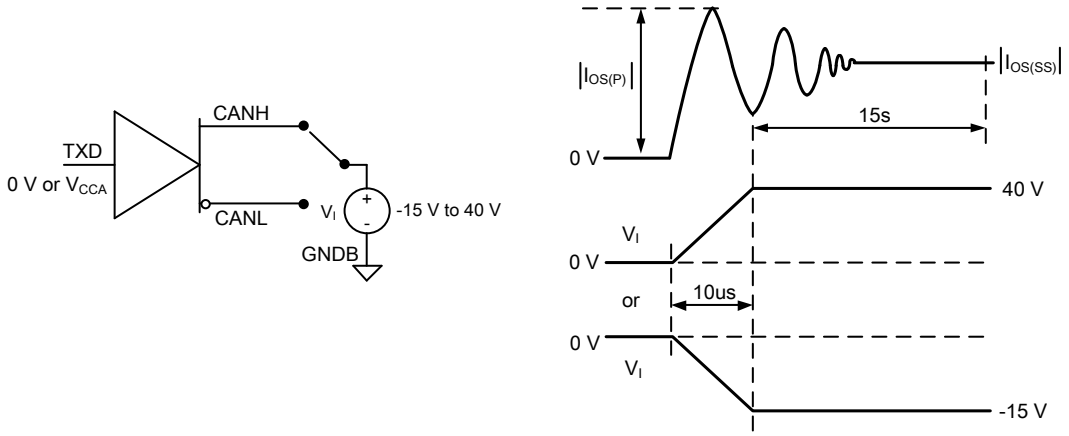


Figure 8-10. Driver Short-Circuit Current Test Circuit and Waveforms

8 Parameter Measurement Information (continued)

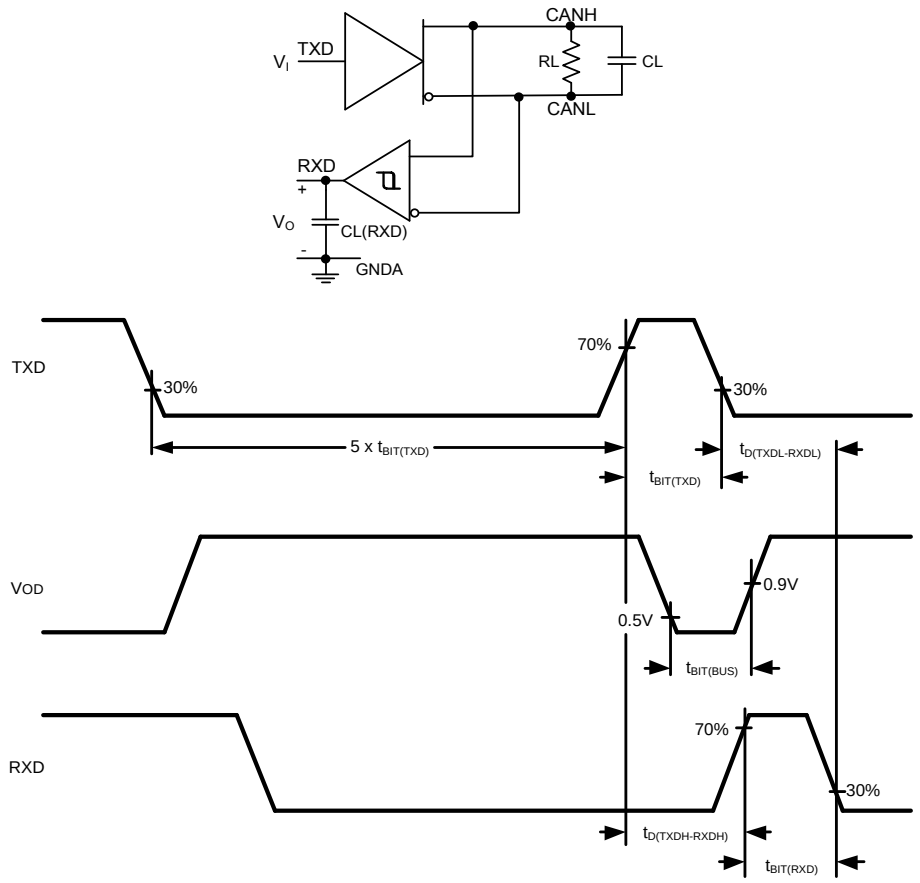
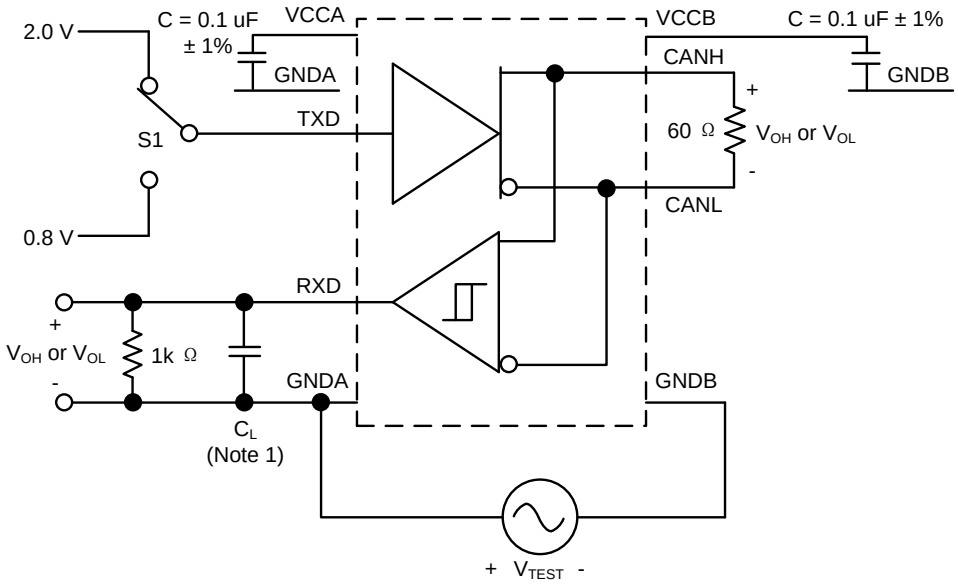


Figure 8-11. CAN FD Timing Parameter Measurement



Note 1: C_L includes probe and jig capacitance.

Figure 8-12. Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The UMISO105x isolated CAN transceivers series provide galvanic isolation of up to 3750 V_{RMS} (DUB8 package) and up to 5000 V_{RMS} (WSOP8/WSOP16 package), and which is fully compatible with the ISO11898-2 standard. Additionally, the devices can achieve efficient and stable communication across isolation barrier with 200kV/μs CMTI and up to 5 Mbps data rate. The logic side power supply is 2.375V to 5.5V which makes the devices ideal for communication with the microcontroller in applications like solar inters, motor control and HVAC systems. The devices are designed for operation in especially harsh environments that feature cross-wire, overvoltage and loss of ground protection from -40 V to 40 V, as well as -15V to 15V common-mode range. The UMISO105x series also feature thermal protection and transmit data dominant time out function.

9.2 CAN Bus States

The CAN bus has two states during operation: dominant and recessive. A dominant bus state, equivalent to logic low, is when the bus is driven differentially by a driver. A recessive bus state, equivalent to a logic high, is when the bus is biased to a common mode of $V_{CCB}/2$. The host microprocessor of the CAN node will transmit and receive data via the bus lines CANH and CANL. The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD.

9.3 Device Functional Modes

Table 9-1. Driver Function Table (Note 1)

V_{CCA}	V_{CCB}	Input	TXD Low-Level Time	Outputs		Bus State
		TXD		CANH	CANL	
Power On	Power On	L	< $t_{DTO(TXD)}$	H	L	Dominant state
		L	> $t_{DTO(TXD)}$	$V_{CCB}/2$	$V_{CCB}/2$	Recessive state
		H or Open	X	$V_{CCB}/2$	$V_{CCB}/2$	Recessive state
Power On	Power Down	X	X	Z	Z	Z
Power Down	Power On	X	X	$V_{CCB}/2$	$V_{CCB}/2$	Recessive state

Note 1: X = Don't care, Z = high impedance.

Table 9-2. Receiver Function Table (Note 1)

$V_{ID} = V_{CANH}-V_{CANL}$	Bus State	RXD
$V_{ID} \geq 0.9V$	Dominant state	L
$0.5V < V_{ID} < 0.9V$	Indeterminate	Indeterminate
$V_{ID} \leq 0.5V$	Recessive state	H
Open	Open	H

Note 1: X = Don't care, Z = high impedance.

9.4 Fail-Safe Features

9.4.1 TXD dominant time-out function

A 'TXD dominant time-out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{DTO(TXD)}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time-out timer is reset when pin TXD is set HIGH.

9.4.2 Overtemperature protection

The output drivers are protected against overtemperature conditions. If the operating junction temperature exceeds the shutdown junction temperature, $T_{J(SD)}$, the output drivers will be disabled until the operating junction temperature falls below $T_{J(SD)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

10 Application Information

10.1 Typical Application

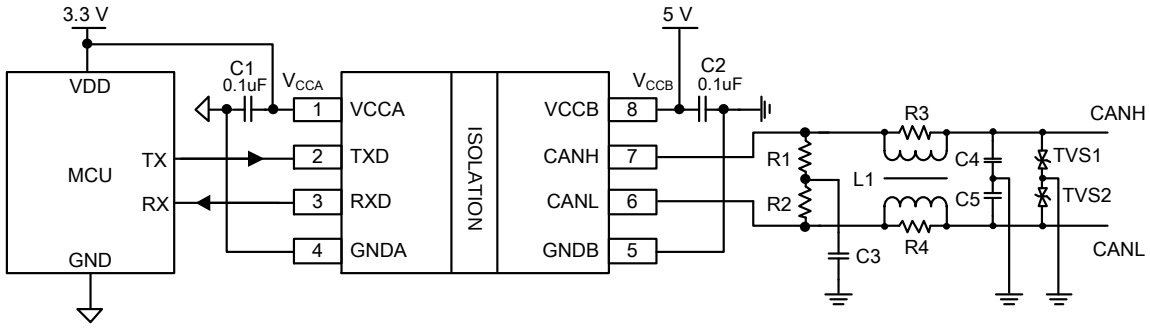
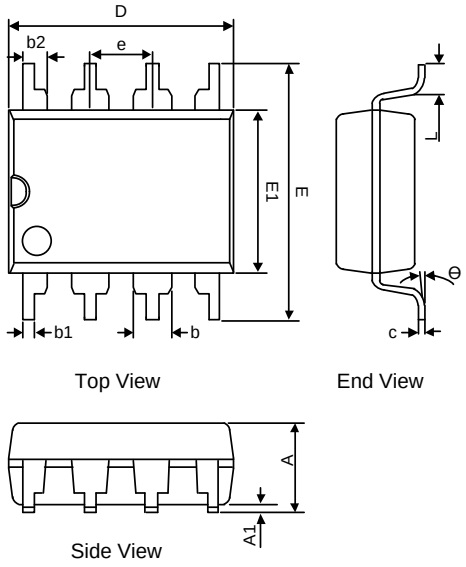


Figure 10-1. UMISO1052 Application Circuit

Package Information

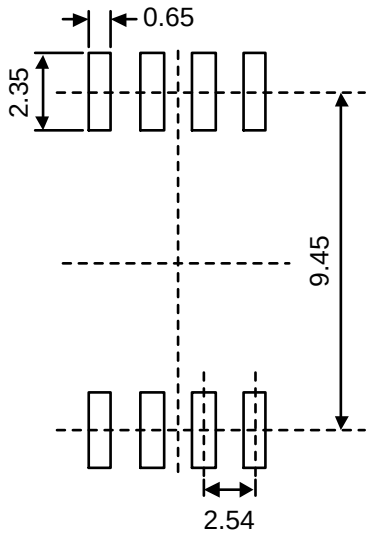
DUB8

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	4.85	-	-	0.194
A1	0.38	-	-	0.015	-	-
b	1.464	1.524	1.584	0.059	0.061	0.064
b1	0.355	-	0.555	0.014	-	0.022
b2	0.93	0.99	1.05	0.037	0.040	0.042
c	0.204	-	0.355	0.008	-	0.014
D	9.02	-	9.55	0.361	-	0.382
E	10.1	-	10.7	0.404	-	0.428
E1	6.37	-	6.87	0.255	-	0.275
e	2.54BSC			0.102BSC		
L	1.15	-	1.45	0.046	-	0.058
θ	0 °	-	8 °	0 °	-	8 °

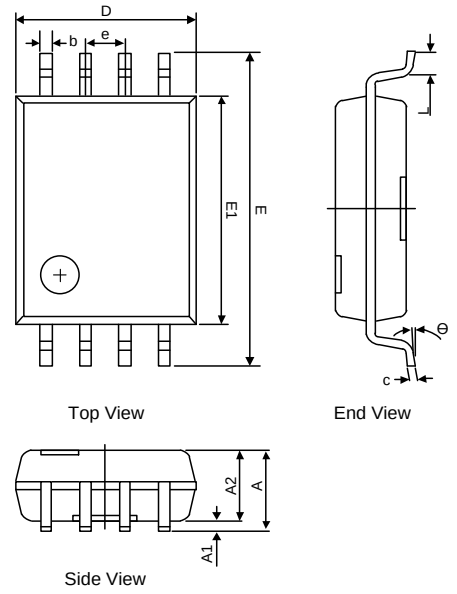
Land Pattern



NOTES:
1. Compound dimension: 9.2×6.62;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

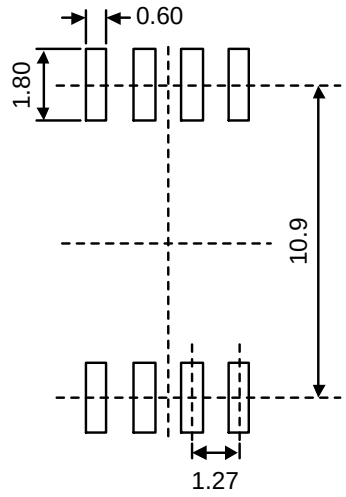
WSOP8

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.80	-	-	0.112
A1	0.36	-	0.46	0.014	-	0.018
A2	2.18	-	2.40	0.087	-	0.096
b	0.31	-	0.51	0.012	-	0.020
c	0.15	-	0.31	0.006	-	0.012
D	5.75	5.85	5.95	0.230	0.234	0.238
E	11.25	11.50	11.75	0.450	0.460	0.470
E1	7.40	7.50	7.60	0.296	0.300	0.304
e	1.27BSC			0.050 BSC		
L	0.50	-	1.00	0.020	-	0.040
θ	0 °	-	8 °	0 °	-	8 °

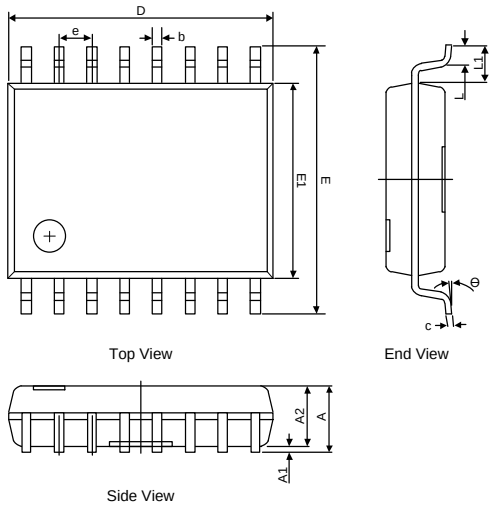
Land Pattern



NOTES:
1. Compound dimension: 5.85×7.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

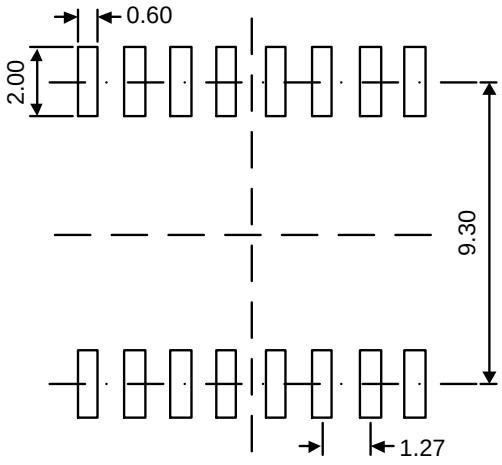
WSOP16

Outline Drawing



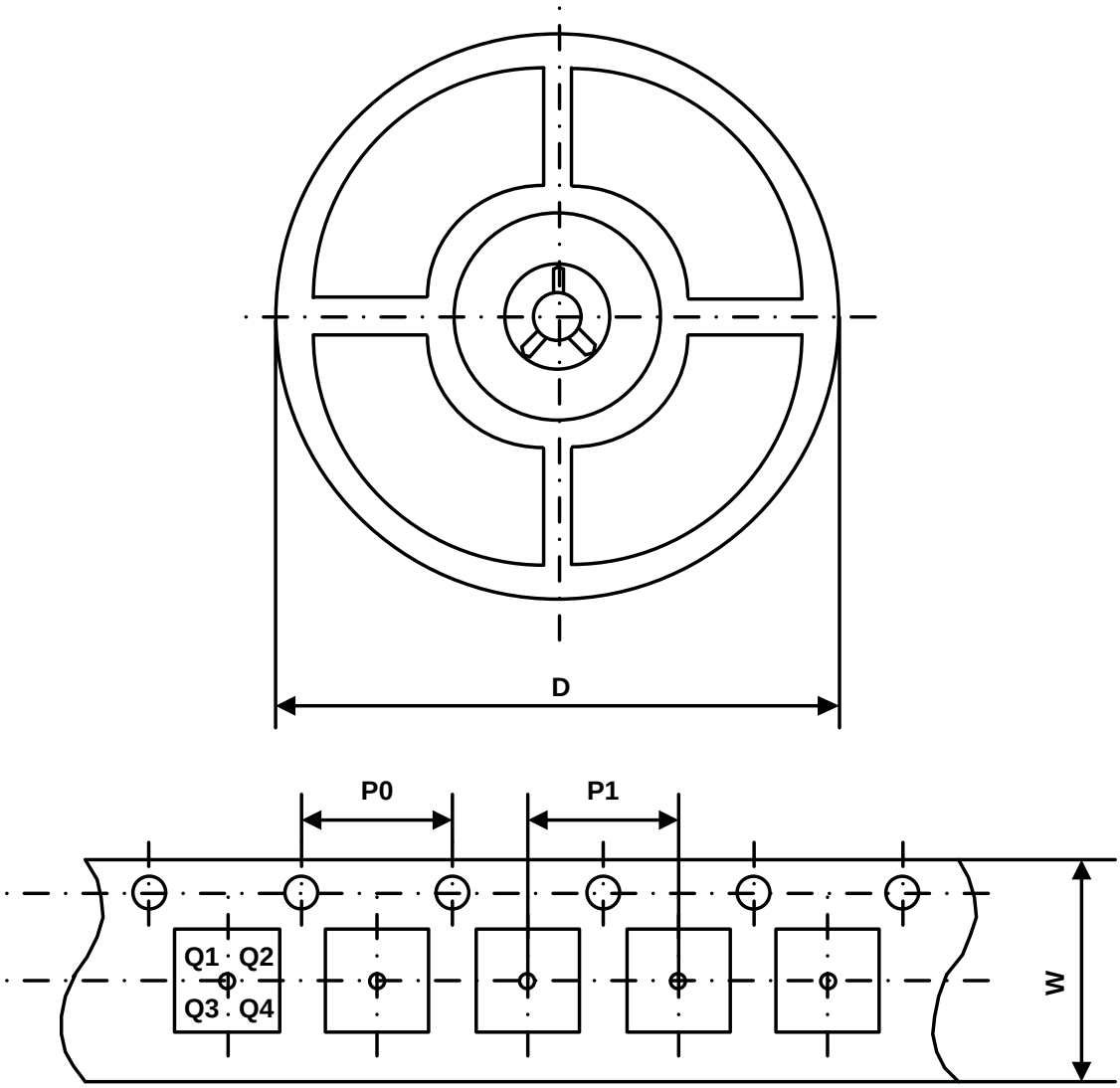
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.65	-	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	2.25	-	2.35	0.089	-	0.093
b	0.35	-	0.43	0.014	-	0.017
c	0.24	-	0.29	0.009	-	0.011
D	10.2	10.3	10.4	0.402	0.406	0.409
E	10.1	10.3	10.5	0.398	0.406	0.413
E1	7.4	7.5	7.6	0.291	0.295	0.299
e	1.27BSC			0.050 BSC		
L	0.55	-	0.85	0.022	-	0.033
L1	1.40REF			0.060REF		
θ	0°	-	8°	0°	-	8°

Land Pattern



NOTES:
1. Compound dimension: 10.30×7.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO1050Z8	DUB8	24 mm	4 mm	16 mm	330 mm	Q1
UMISO1050WS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO1050WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO1052WS8	WSOP8	16 mm	4 mm	16 mm	330 mm	Q1
UMISO1052WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1

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