4-Bits Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

UMLSF0204 *TSSOP14/CSP12 1.9×1.4/QFN12 1.7×2.0/QFN14 3.5×3.5*
UMLSF0204D *TSSOP14/CSP12 1.9×1.4/QFN12 1.7×2.0/QFN14 3.5×3.5*

1 Description

The UMLSF0204 series operate from 0.8 V to 4.5 V (V_{REF_A}) and 1.8 V to 5.5 V (V_{REF_B}). This range allows for bidirectional voltage translations between 0.8 V and 5.0 V without the need for a direction terminal in open-drain or push-pull applications. The device supports speed greater than 100MHz (200Mbps) for open-drain systems with 15 pF capacitive load and 165Ω pull-up resistor.

When the An or Bn port is low, the switch is in the On-state and a low resistance connection exists between the An and Bn ports. The low R_{ON} of the switch allows minimal propagation delay and signal distortion. The voltage on the A or B side will be limited to V_{REF_A} and can be pulled up to any level between V_{REF_A} and 5 V. The ability to set up different voltage translation levels on each channel allows a seamless translation between higher and lower voltages selected by the user without the need for a direction pin which minimizes system effort.

The EN pin of the UMLSF0204 is high, the translator switch is on, and the An I/O is connected to the Bn I/O. On the contrary, the EN pin of the UMLSF0204D is low-active.

The UMLSF0204 series are available in CSP12 1.9×1.4, QFN12 1.7×2.0, QFN14 3.5×3.5 and TSSOP14 packages.

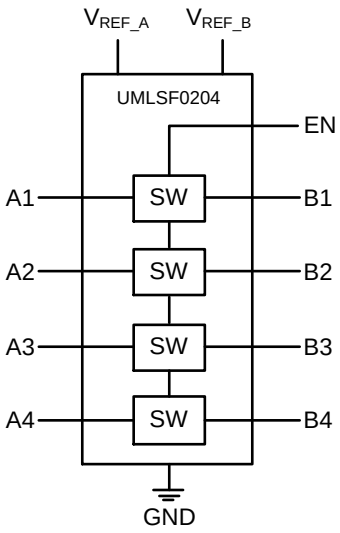
2 Features

- Bidirectional voltage translation with no direction pin
- I_{OFF} supports partial power-down mode operation
- Allow bidirectional voltage level translation between:
  - 0.8 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.2 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.8 V ↔ 2.5, 3.3, 5 V
  - 2.5 V ↔ 3.3, 5 V
  - 3.3 V ↔ 5 V
- ESD protection exceeds JESD22
  - ±5000V Human body model
  - ±2000V Charged-device model
- Up translation
  - ≤ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≤ 40MHz (80Mbps); C_L = 50 pF
- Down translation
  - ≥ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≥ 40MHz (80Mbps); C_L = 50 pF
- Low standby current
- 5 V Tolerance I/O port to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O terminals when EN is not activated
- Latch-up performance exceeds 200 mA per JESD 78, Class II

3 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C and other interfaces in telecom infrastructure
- Personal computing
- Industrial
- Automotive

4 Simplified Schematic

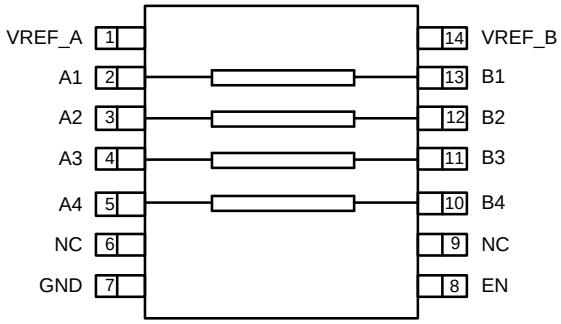


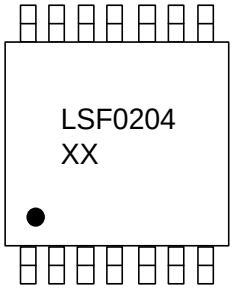
5 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UMLSF0204UE	LSF0204	TSSOP14	3000pcs/13Inch Tape & Reel
UMLSF0204H	EBE	CSP12 1.9×1.4	3000pcs/7Inch Tape & Reel
UMLSF0204QA	APD	QFN12 1.7×2.0	3000pcs/7Inch Tape & Reel
UMLSF0204QS	UMLSF0204	QFN14 3.5×3.5	3000pcs/7Inch Tape & Reel
UMLSF0204DUE	LSF0204D	TSSOP14	3000pcs/13Inch Tape & Reel
UMLSF0204DH	EBF	CSP12 1.9×1.4	3000pcs/7Inch Tape & Reel
UMLSF0204DQA	APE	QFN12 1.7×2.0	3000pcs/7Inch Tape & Reel
UMLSF0204DQS	UMLSF0204D	QFN14 3.5×3.5	3000pcs/7Inch Tape & Reel

6 Pin Configuration and Function

(Top View)





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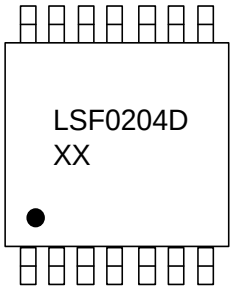
TSSOP14



XX: Week Code
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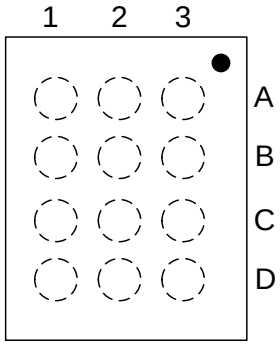
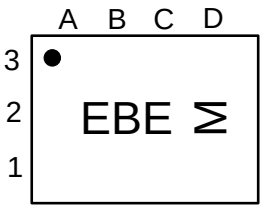
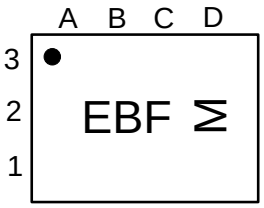
TSSOP14

(Top View)





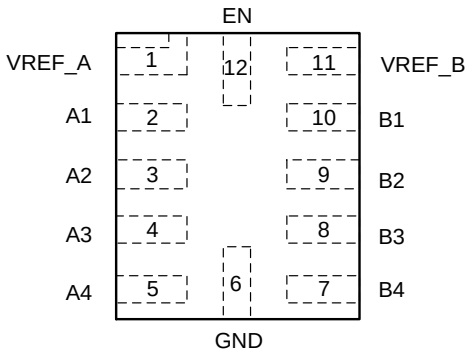
M: Month Code
UMLSF0204H
CSP12 1.9×1.4



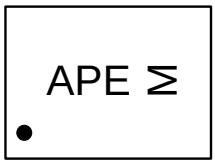
M: Month Code
UMLSF0204DH
CSP12 1.9×1.4

6 Pin Configuration and Function (continued)

(Top View)

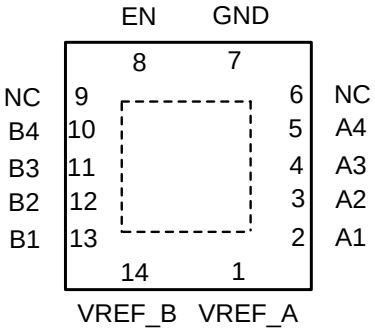


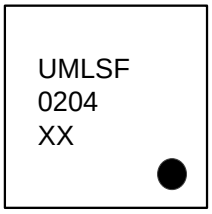
M: Month Code
UMLSF0204QA
QFN12 1.7×2.0



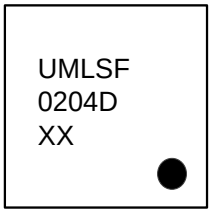
M: Month Code
UMLSF0204DQA
QFN12 1.7×2.0

(Top View)





XX: Week Code
UMLSF0204QS
QFN14 3.5×3.5



XX: Week Code
UMLSF0204DQS
QFN14 3.5×3.5

6 Pin Configuration and Function (continued)

6.1 Mapping for UMLSF0204H and UMLSF0204DH

Transparent Top View

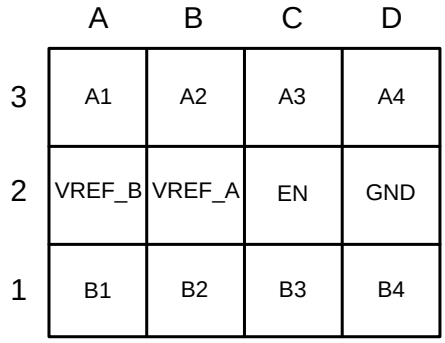


Table 6-1. Pin Functions

Pin Name	Function
VREF_A	Reference supply voltage.
A1	Input/output 1.
A2	Input/output 2.
A3	Input/output 3.
A4	Input/output 4.
GND	Ground.
EN	Switch enable input. Referenced to V_{REF_A}. EN is high-active for UMLSF0204; EN is low-active for UMLSF0204D.
NC	No connection. Not internally connected.
B4	Input/output 4.
B3	Input/output 3.
B2	Input/output 2.
B1	Input/output 1.
VREF_B	Reference supply voltage.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Value	Unit
V_I	Input Voltage (Note 2)		-0.5 to +7	V
$V_{I/O}$	Input/output voltage (Note 2)		-0.5 to +7	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001		±5000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101		±2000	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
T_J	Operating Junction Temperature		-40 to +150	℃
T_{STG}	Storage Temperature		-65 to +150	℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 Recommended Operating Conditions

Over recommended operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Min	Max	Unit
$V_{I/O}$	Input/output voltage	0	5.5	V
$V_{REF\_A/B/EN}$	Reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	-40	125	℃

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TSSOP14	156.9	℃/W
		CSP12 1.9×1.4	82.7	
		QFN12 1.7×2.0	194.8	
		QFN14 3.5×3.5	82.2	
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	TSSOP14	81.3	℃/W
		CSP12 1.9×1.4	0.6	
		QFN12 1.7×2.0	97.7	
		QFN14 3.5×3.5	97.2	
$R_{\theta JB}$	Junction-to-board thermal resistance	TSSOP14	99	℃/W
		CSP12 1.9×1.4	22.7	
		QFN12 1.7×2.0	121.6	
		QFN14 3.5×3.5	59.2	

7.4 Electrical Characteristics (Note 1)

Over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Test Conditions	Min	Typ	Max	Unit
V_{IK}		I_I = -18 mA, V_{EN} = 0 V			-1.2	V
I_{IH}		V_I = 5 V, V_{EN} = 0 V			5	μA
I_{CCBA} (Note 2)	Leakage from V_{REF_B} to V_{REF_A}	V_{REF_B} = 3.3 V, V_{REF_A} = 1.8 V, V_{EN} = V_{REF_A}, I_O = 0, V_I = 3.3 V or GND		2.8	10	μA
I_{CCA}+I_{CCB}	Total Current through GND	V_{REF_B} = 3.3 V, V_{REF_A} = 1.8 V, V_{EN} = V_{REF_A}, I_O = 0, V_I = 3.3 V or GND		0.2		μA
I_{IN}	Control pin current	V_{REF_B} = 5.5 V, V_{REF_A} = 4.5 V, V_{EN} = 0 V to V_{REF_A}, I_O = 0 V			±1	μA
I_{OFF}	Power Off Leakage Current	V_{REF_B} = V_{REF_A} = 0 V, V_{EN} = GND, I_O = 0 , V_I = 5 V or GND		0.3	±3.5	μA
$C_{I(REF\_A/B/EN)}$		V_I = 3 V or 0 V		9		pF
$C_{IO(OFF)}$		V_O = 3 V or 0 V, V_{EN} = 0 V		4.5	6	pF
$C_{IO(ON)}$		V_O = 3 V or 0 V, V_{EN} = V_{REF_A}		9.5	13	pF
V_{IH}	High-level input voltage for EN pin	V_{REF_A} = 1.5 V to 4.5 V	0.7× V_{REF_A}			V
V_{IL}	Low-level input voltage for EN pin	V_{REF_A} = 1.5 V to 4.5 V			0.3× V_{REF_A}	V
V_{IH}	High-level input voltage for EN pin	V_{REF_A} = 1.0 V to 1.5 V	0.8× V_{REF_A}			V
V_{IL}	Low-level input voltage for EN pin	V_{REF_A} = 1.0 V to 1.5 V			0.3× V_{REF_A}	V
Δ t/Δ v	Input transition rise or fall rate for EN pin			10		ns/V
R_{ON} (Note 3)		V_I = 0 V, I_O = 64 mA, V_{REF_A} = V_{EN} = 3.3 V; V_{REF_B} = 5 V		3		Ω
		V_I = 0 V, I_O = 64 mA, V_{REF_A} = V_{EN} = 1.8 V; V_{REF_B} = 5 V		4		
		V_I = 0 V, I_O = 32 mA, V_{REF_A} = V_{EN} = 1.0 V; V_{REF_B} = 5 V		8		

7.4 Electrical Characteristics (Note 1) (continued)

Over recommended operating free-air temperature range (unless otherwise noted).

Parameter	Test Conditions	Min	Typ	Max	Unit
R_{ON} (Note 3)	V_I = 0 V, I_O = 32 mA, V_{REF_A} = V_{EN} = 1.8 V; V_{REF_B} = 5 V		4		Ω
	V_I = 0 V, I_O = 32 mA, V_{REF_A} = V_{EN} = 2.5 V; V_{REF_B} = 5 V		4		
	V_I = 1.8 V, I_O = 15 mA, V_{REF_A} = V_{EN} = 3.3 V; V_{REF_B} = 5 V		5		
	V_I = 1.0 V, I_O = 10 mA, V_{REF_A} = V_{EN} = 1.8 V; V_{REF_B} = 3.3 V		10		
	V_I = 0 V, I_O = 10 mA, V_{REF_A} = V_{EN} = 1.0 V; V_{REF_B} = 3.3 V		6		
	V_I = 0 V, I_O = 10 mA, V_{REF_A} = V_{EN} = 1.0 V; V_{REF_B} = 1.8 V		6.5		

Note 1: All typical values are at T_A = 25°C.
Note 2: The actual supply current for UMLSF0204 is I_{CCA} + I_{CCB}; the leakage from V_{REF_B} to V_{REF_A} can be measured on V_{REF_A} and V_{REF_B} pin.
Note 3: Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.5 Switching Characteristics: Translating Down, 3.3 V to 1.8 V

V_{REF_A} = 1.8 V, V_{REF_B} = 3.3 V, V_{EN} = 1.8 V, V_{PU_1} = 3.3 V, V_{PU_2} = 1.8 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V, V_M = 1.15 V. Over recommended operating free-air temperature range (unless otherwise noted).

Parameter	From (Input)	To (Output)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A or B	B or A	0.8	5.49	0.5	5.29	0.3	5.19	ns
t_{PHL}			0.9	4.9	0.7	4.7	0.5	4.5	ns
t_{PLZ}			8.4	18	8.4	16.5	8.3	15	ns
t_{PZL}			6.5	45	6.4	40	6.3	37	ns
f_{MAX}			50		100		100		MHz

7.5 Switching Characteristics (continued): Translating Down, 3.3 V to 1.2 V

V_{REF_A} = 1.2 V, V_{REF_B} = 3.3 V, V_{EN} = 1.2 V, V_{PU_1} = 3.3 V, V_{PU_2} = 1.2 V, R_L = NA, V_{IH} = 3.3 V, V_{IL} = 0 V, V_M = 0.85 V. Over recommended operating free-air temperature range (unless otherwise noted).

Parameter	From (Input)	To (Output)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A or B	B or A	1.1	4.1	0.7	3.9	0.4	3.8	ns
t_{PHL}			0.8	4.7	0.7	4.5	0.5	4.3	ns
f_{MAX}			50		100		100		MHz

7.5 Switching Characteristics (continued): Translating Up, 1.8 V to 3.3 V

V_{REF_A} = 1.8 V, V_{REF_B} = 3.3 V, V_{EN} = 1.8 V, V_{PU_1} = 3.3 V, V_{PU_2} = 1.8 V, R_L = 500 Ω, V_{IH} = 1.8 V, V_{IL} = 0 V, V_M = 0.9 V. Over recommended operating free-air temperature range (unless otherwise noted).

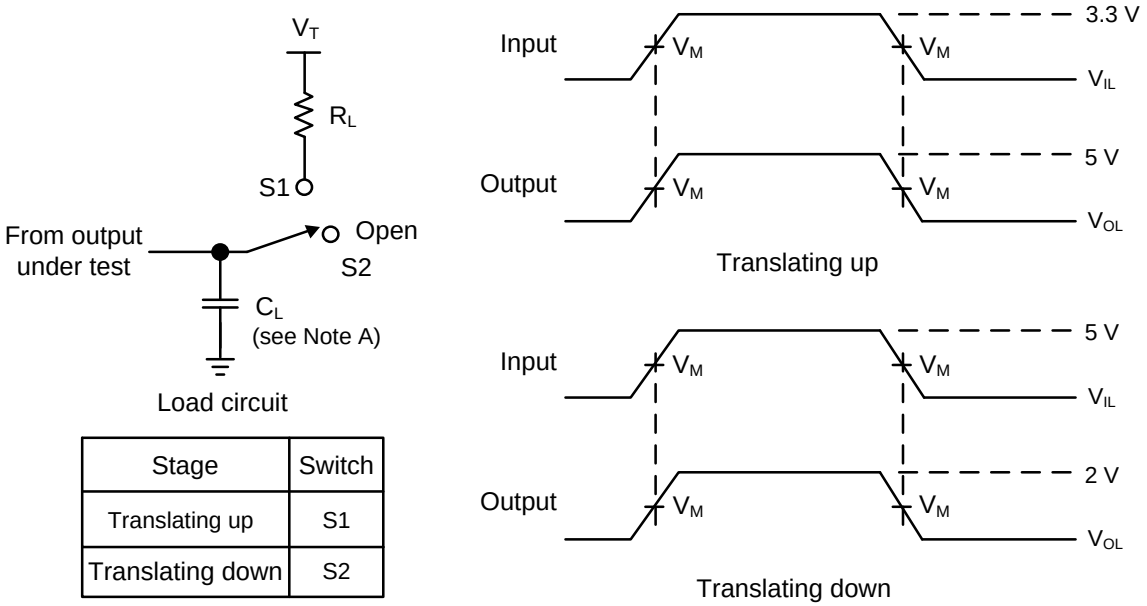
Parameter	From (Input)	To (Output)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A or B	B or A	0.6	5.7	0.4	5.3	0.1	5.13	ns
t_{PHL}			1.6	6.7	1.2	6.4	0.8	5.3	ns
t_{PLZ}			10.3	18	9.4	16.5	9	15	ns
t_{PZL}			13.4	45	11.5	40	9.8	37	ns
f_{MAX}			50		100		100		MHz

7.5 Switching Characteristics (continued): Translating Up, 1.2 V to 1.8 V

V_{REF_A} = 1.2 V, V_{REF_B} = 1.8 V, V_{EN} = 1.2 V, V_{PU_1} = 1.8 V, V_{PU_2} = 1.2 V, R_L = 500 Ω, V_{IH} = 1.2 V, V_{IL} = 0 V, V_M = 0.6 V. Over recommended operating free-air temperature range (unless otherwise noted).

Parameter	From (Input)	To (Output)	C_L = 50 pF		C_L = 30 pF		C_L = 15 pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
t_{PLH}	A or B	B or A	0.8	7.25	0.5	7.05	0.2	6.85	ns
t_{PHL}			1.8	7.03	1.4	6.5	1	5.4	ns
f_{MAX}			50		100		100		MHz

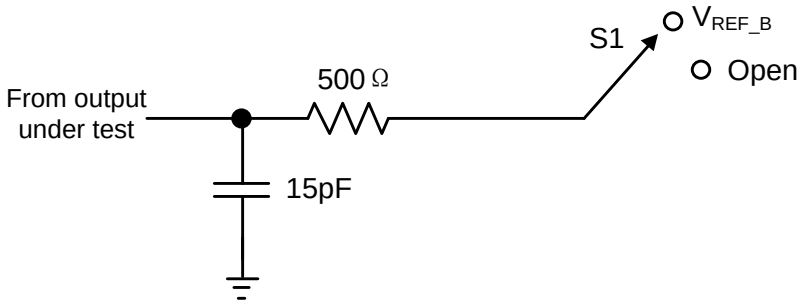
8 Parameter Measurement Information



Stage	Switch
Translating up	S1
Translating down	S2

Note 1: C_L includes probe and jig capacitance.
Note 2: All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2 ns, t_F ≤ 2 ns.
Note 3: The outputs are measured one at a time, with one transition per measurement.

Figure 8-1. Load Circuit for Outputs



Test	S1
t_{PZL}/t_{PLZ}	V_{REF_B}

Figure 8-2. Load Circuit for Enable/Disable Time Measurement

8 Parameter Measurement Information (continued)

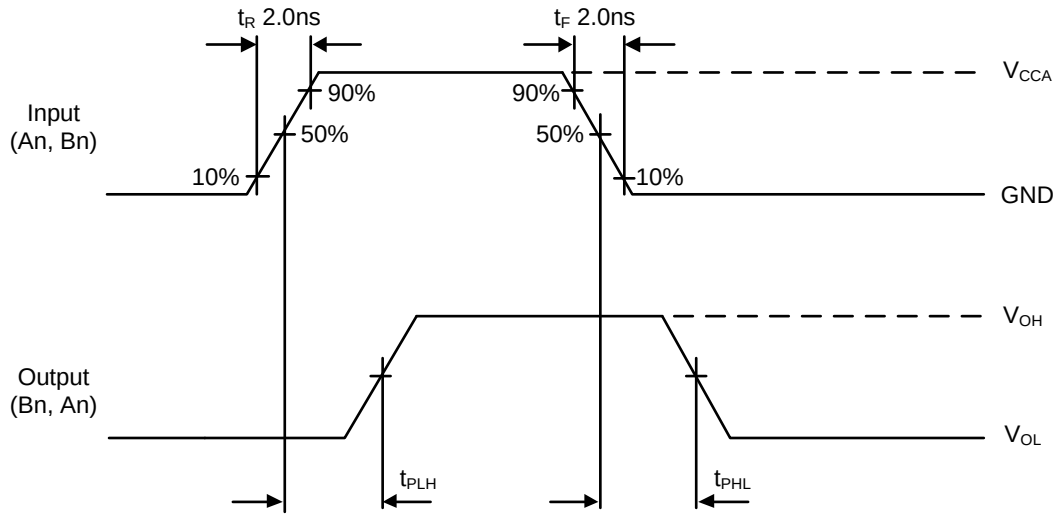


Figure 8-3. Voltage Waveforms t_{PLH}, t_{PHL}

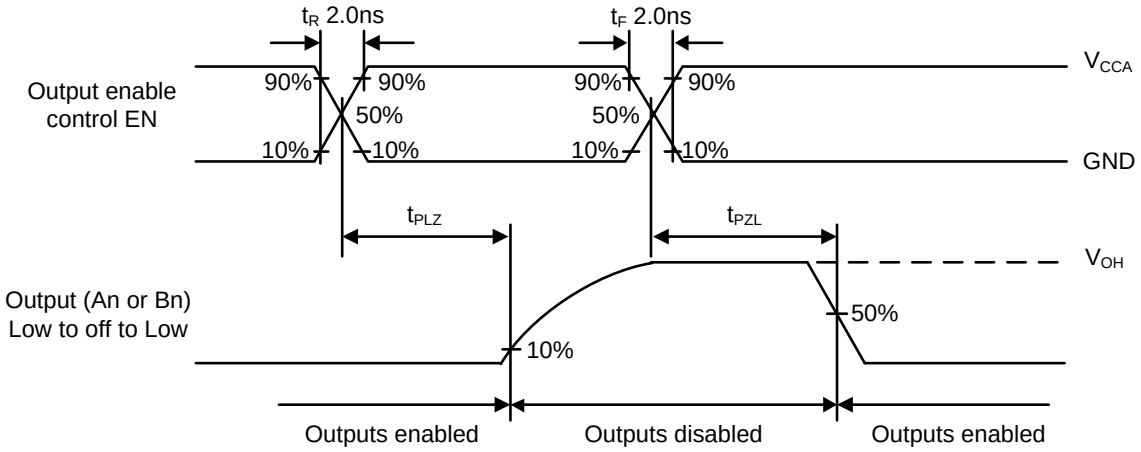


Figure 8-4. Voltage Waveforms t_{PLZ}, t_{PZL}

9 Detailed Description

9.1 Overview

The UMLSF0204 series may be used in level translation applications for interfacing devices or systems operating at different interface voltages with one another. The devices are ideal for use in applications where an open-drain driver is connected to the data I/Os. The devices can achieve 100 MHz with the appropriate pull-up resistors and layout. What's more, the UMLSF0204 may also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram

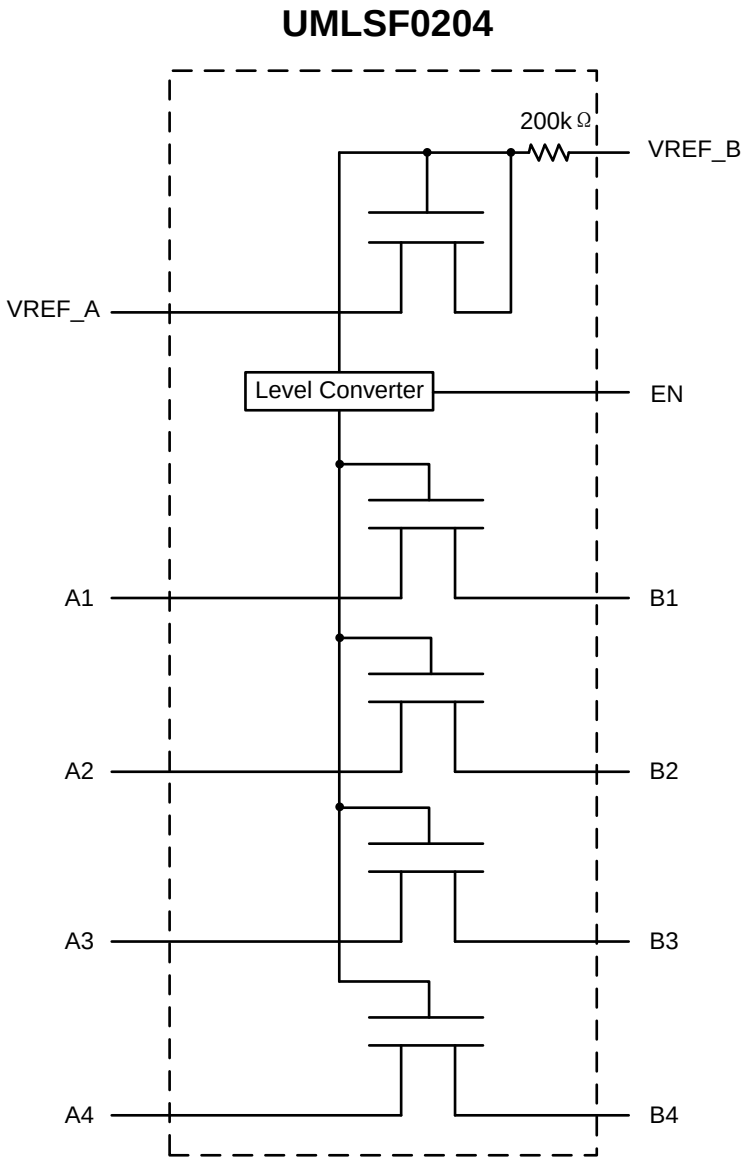


Figure 9-1. UMLSF0204 Block Diagram

10 Feature Description

10.1 Support High Speed Translation, Greater than 100MHz

The UMLSF0204 series support more consumer or telecom interfaces (MDIO or SDIO).

10.2 Bidirectional Voltage Translation Without DIR Terminal

The UMLSF0204 series support automatic direction voltage translation that minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I^2C, or SMbus).

10.3 5V Tolerance on IO Port and 125°C Support

The UMLSF0204 series feature 5V tolerance and -40°C to 125°C operating temperature range that compliant with TTL levels in industrial and telecom applications.

10.3 I_{OFF} Supports Partial Power Down Mode Operation

When V_{REF_A}, V_{REF_B} = 0, all of data pins and EN pin are Hi-Z, inhibiting current backflow into the device.
EN logic circuit is supplied by V_{REF_A}, once V_{REF_A} power up first and all of data pins are unknown state until V_{REF_B} and EN ready. No power sequence is required to enable UMLSF0204 and operate function normally.

10.4 Functional Modes

Table 10-1 lists the device functional modes of the UMLSF0204x.

Table 10-1. Function Table

Input EN terminal	Function	
	UMLSF0204	UMLSF0204D
H	An, Bn channel Enabled	Hi-Z
L	Hi-Z	An, Bn channel Enabled

11 Application Information

11.1 Application Information

The UMLSF0204 series are suitable for open-drain or push-pull interface like GPIO, SPI. MDIO, SMBus, PMBus, I²C, UART, SVID.

11.2 Typical Applications

The UMLSF0204 series are suitable for open-drain or push-pull interface like GPIO, SPI. MDIO, SMBus, PMBus, I²C, UART, SVID.

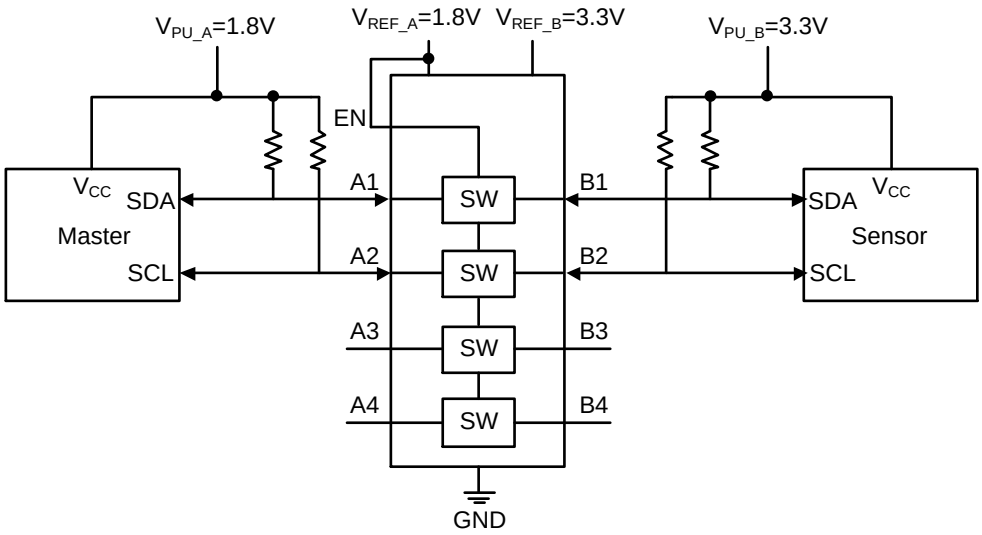
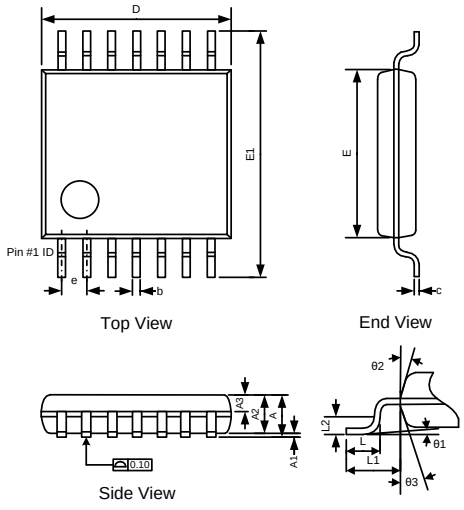


Figure 11-1. UMLSF0204 I²C Bidirectional Translation

Package Information

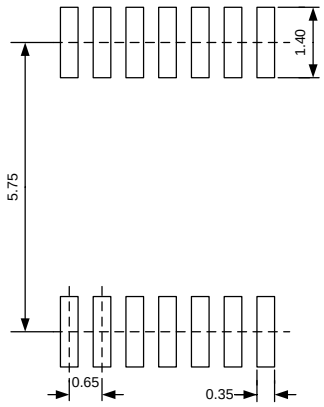
TSSOP14

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.90	1.00	1.05	0.035	0.039	0.041
A3	0.34	0.44	0.54	0.013	0.017	0.021
b	0.20	-	0.28	0.008	-	0.011
c	0.10	-	0.19	0.004	-	0.007
D	4.86	4.96	5.06	0.191	0.195	0.199
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
L2	0.25BSC			0.010BSC		
θ1	0 °	-	8 °	0 °	-	8 °
θ2	10 °	12 °	14 °	10 °	12 °	14 °
θ3	10 °	12 °	14 °	10 °	12 °	14 °

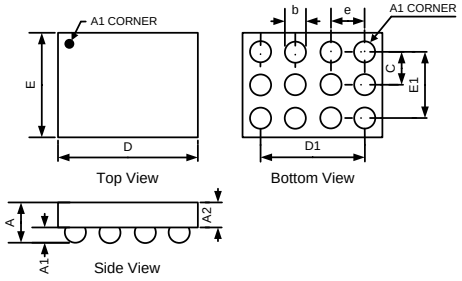
Land Pattern



NOTES:
1. Compound dimension: 4.96×4.40;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

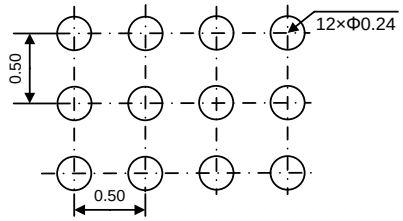
CSP12 1.9×1.4

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	0.68	-	-	0.027
A1	0.21	0.231	0.24	0.0083	0.0091	0.0094
A2	0.40	0.42	0.44	0.0157	0.0165	0.0173
b	0.27	0.30	0.32	0.011	0.012	0.013
C	0.50TYP			0.020TYP		
D	1.82	-	1.90	0.072	-	0.075
D1	1.50TYP			0.059TYP		
E	1.32	-	1.40	0.052	-	0.055
E1	1.00TYP			0.039TYP		
e	0.50TYP			0.020TYP		

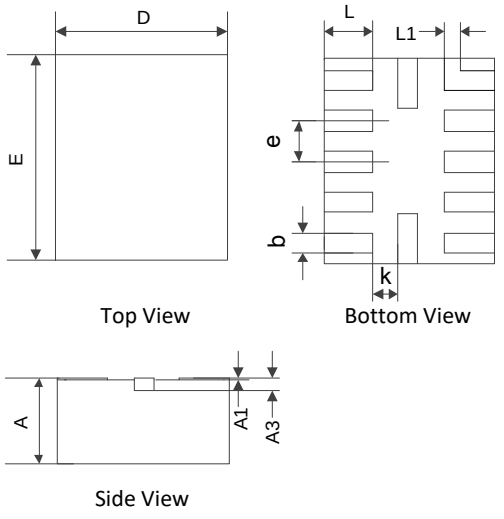
Land Pattern



NOTES:
1. Bump is Lead Free Sn/Ag/Cu.
2. Unit: mm.
3. Non-solder mask defined copper landing pad.
4. Laser Mark on silicon die back; back-lapped.

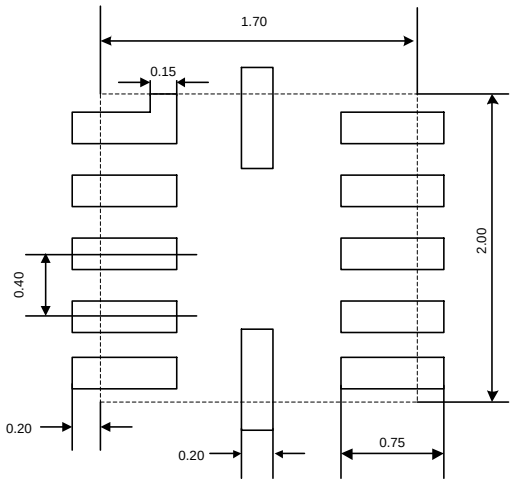
QFN12 1.7×2.0

Outline Drawing



Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	-	0.05	0.000	-	0.002
A3	0.152REF			0.006REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.60	1.70	1.80	0.063	0.067	0.071
E	1.90	2.00	2.10	0.075	0.079	0.083
e	0.40TYP			0.016TYP		
k	0.25REF			0.010REF		
L	0.40	0.50	0.60	0.016	0.020	0.024
L1	0.150REF			0.006REF		

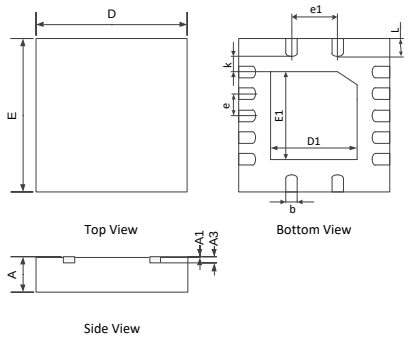
Land Pattern



NOTES:
1. Compound dimension: 1.7×2.0 ;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

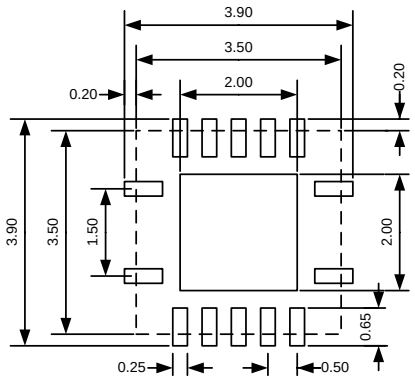
QFN14 3.5×3.5

Outline Drawing



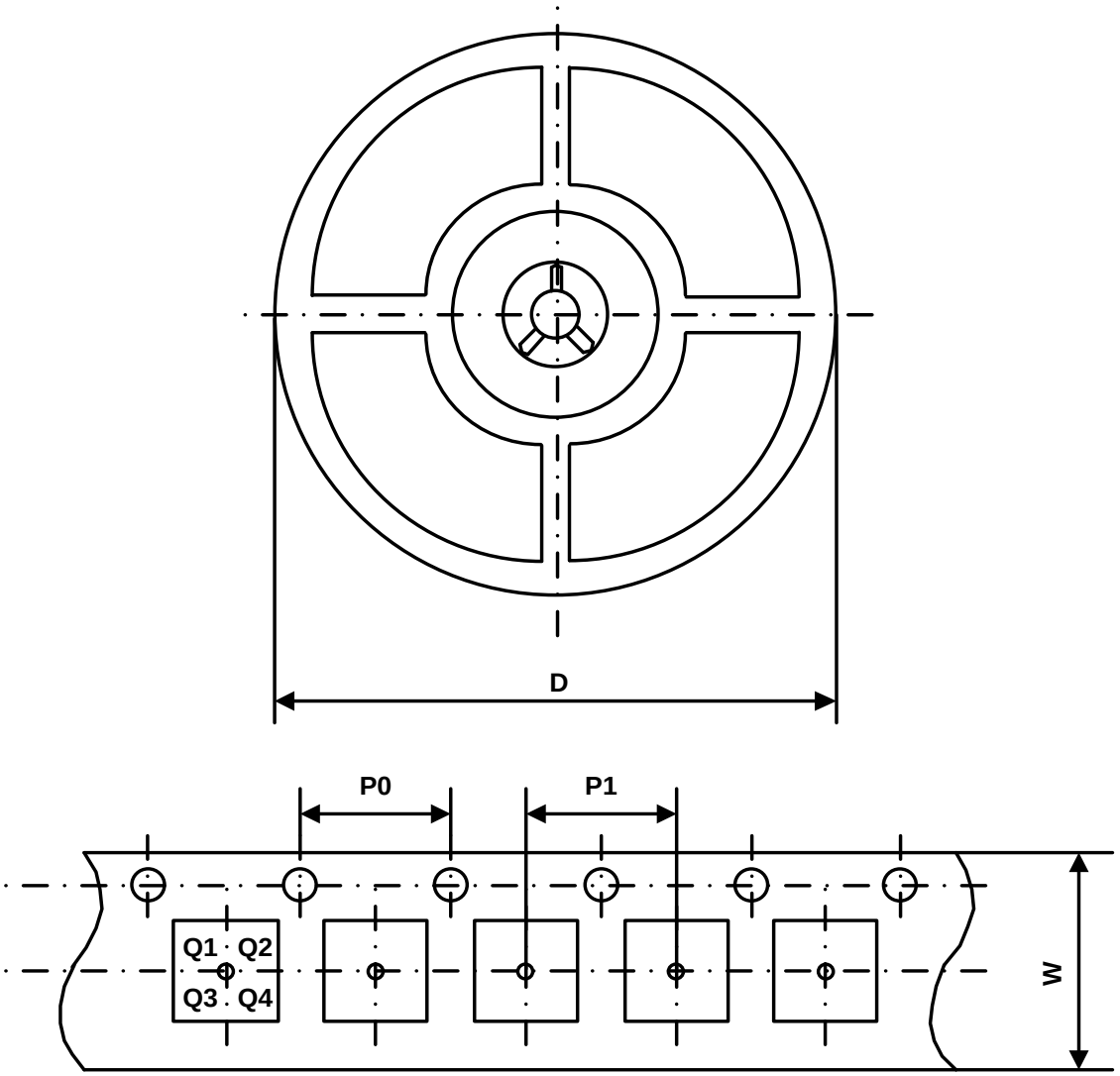
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.700	-	0.850	0.028	-	0.031
A1	0.000	0.02	0.050	0.000	0.0008	0.002
A3	0.203REF			0.008REF		
D	3.424	3.500	3.576	0.135	0.138	0.141
E	3.424	3.500	3.576	0.135	0.138	0.141
D1	1.900	-	2.150	0.077	-	0.085
E1	1.900	-	2.150	0.077	-	0.085
k	0.200MIN			0.008MIN		
b	0.200	0.250	0.300	0.008	0.010	0.012
e	0.500TYP			0.020TYP		
e1	1.500TYP			0.059TYP		
L	0.324	-	0.476	0.013	-	0.019

Land Pattern



NOTES:
1. Compound dimension: 3.50×3.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMLSF0204UE	TSSOP14	16 mm	4 mm	8 mm	330 mm	Q1
UMLSF0204H	CSP12 1.9×1.4	8 mm	4 mm	4 mm	180 mm	Q2
UMLSF0204QA	QFN12 1.7×2.0	8 mm	4 mm	4 mm	180 mm	Q1
UMLSF0204QS	QFN14 3.5×3.5	12 mm	4 mm	8 mm	330 mm	Q1
UMLSF0204DUE	TSSOP14	16 mm	4 mm	8 mm	330 mm	Q1
UMLSF0204DH	CSP12 1.9×1.4	8 mm	4 mm	4 mm	180 mm	Q2
UMLSF0204DQA	QFN12 1.7×2.0	8 mm	4 mm	4 mm	180 mm	Q1
UMLSF0204DQS	QFN14 3.5×3.5	12 mm	4 mm	8 mm	330 mm	Q1

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