8-Bit Auto-Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

UMLSF0108UK ***TSSOP20***
UMLSF0108QCK ***QFN20 4.5×2.5***

1 Description

The UMLSF0108 operates from 0.8 V to 4.5 V (V_{REF_A}) and 1.65 V to 5.5 V (V_{REF_B}). The device supports bidirectional voltage translations between 0.8 V and 5.0 V without the need for a direction terminal in open-drain or push-pull applications. The UMLSF0108 supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up to 40MHz up or down translation at 50pF capacitive load.

When the An or Bn port is low, the switch is in the On-state and a low resistance connection exists between the An and Bn ports. The low R_{ON} of the switch allows minimal propagation delay and signal distortion. The voltage on the A or B side will be limited to V_{REF_A} and can be pulled up to any level between V_{REF_A} and 5 V. The ability to set up different voltage translation levels on each channel allows a seamless translation between higher and lower voltages selected by the user without the need for a direction pin which minimizes system effort.

The UMLSF0108 series are available in TSSOP20 and QFN20 4.5×2.5 packages.

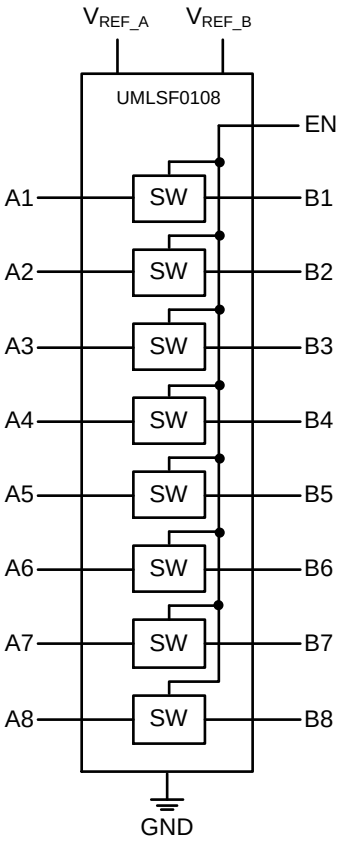
2 Features

- Bidirectional voltage translation with no direction pin
- I_{OFF} supports partial power-down mode operation
- Allow bidirectional voltage level translation between:
  - 0.8 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.2 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.8 V ↔ 2.5, 3.3, 5 V
  - 2.5 V ↔ 3.3, 5 V
  - 3.3 V ↔ 5 V
- ESD protection
  - ±4000V Human body model
  - ±2000V Charged-device model
- Up translation
  - ≤ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≤ 40MHz (80Mbps); C_L = 50 pF
- Down translation
  - ≥ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≥ 40MHz (80Mbps); C_L = 50 pF
- Low standby current
- 5 V Tolerance I/O port to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O pins when EN is low
- Operating temperature range: -40°C to 125°C
- Latch-up performance exceeds 200 mA per JESD 78, Class II

3 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C and other interfaces in telecom infrastructure
- Personal computing
- Industrial
- Automotive

4 Simplified Schematic

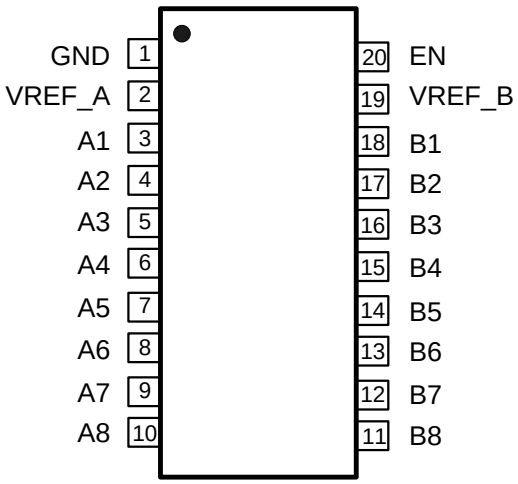


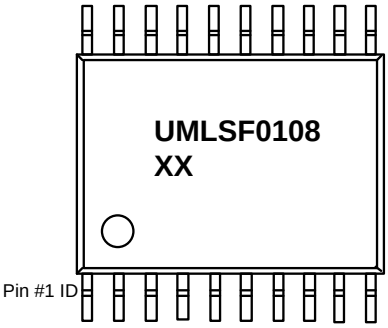
5 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UMLSF0108UK	UMLSF0108	TSSOP20	3000pcs/13Inch Tape & Reel
UMLSF0108QCK	LSF0108	QFN20 4.5×2.5	3000pcs/13Inch Tape & Reel

6 Pin Configuration and Function

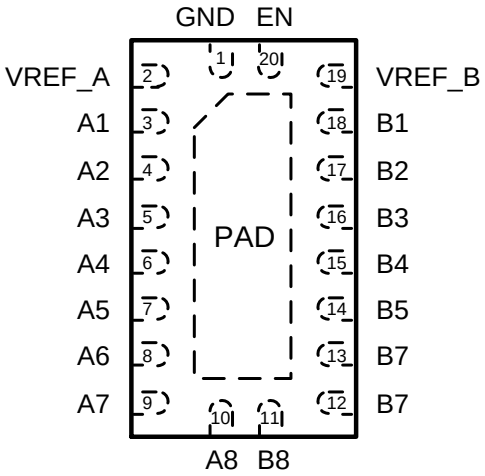
(Top View)

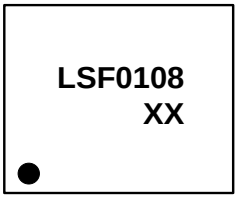




XX: Week Code
UMLSF0108UK
TSSOP20

(Top View)





XX: Week Code
UMLSF0108QCK
QFN20 4.5×2.5

6 Pin Configuration and Function (continued)

Table 6-1. Pin Functions

Pin No.	Pin Name	Function
1	GND	Ground.
2	VREF_A	Reference supply voltage.
3	A1	Input/output 1.
4	A2	Input/output 2.
5	A3	Input/output 3.
6	A4	Input/output 4.
7	A5	Input/output 5.
8	A6	Input/output 6.
9	A7	Input/output 7.
10	A8	Input/output 8.
11	B8	Input/output 8.
12	B7	Input/output 7.
13	B6	Input/output 6.
14	B5	Input/output 5.
15	B4	Input/output 4.
16	B3	Input/output 3.
17	B2	Input/output 2.
18	B1	Input/output 1.
19	VREF_B	Reference supply voltage.
20	EN	Enable input; connect to V_{REF_B} and pull-up through a high resistor (200kΩ).

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Value	Unit
V_I	Input Voltage (Note 2)		-0.5 to +7	V
$V_{I/O}$	Input/output voltage (Note 2)		-0.5 to +7	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001		±4000	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002		±2000	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
T_J	Operating Junction Temperature		-40 to +150	℃
T_{STG}	Storage Temperature		-65 to +150	℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 Recommended Operating Conditions

Over recommended operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Min	Max	Unit
$V_{I/O}$	Input/output voltage (An, Bn pins)	0	5.5	V
$V_{REF\_A/B/EN}$	Reference voltage	0	5.5	V
I_{PASS}	Pass transistor current		64	mA
T_A	Operating free-air temperature	-40	125	℃

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TSSOP20	108.8	℃/W
		QFN20 4.5×2.5	74.3	
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	TSSOP20	45.7	℃/W
		QFN20 4.5×2.5	76.6	
$R_{\theta JB}$	Junction-to-board thermal resistance	TSSOP20	61.8	℃/W
		QFN20 4.5×2.5	46.6	

7.4 Electrical Characteristics (Note 1)

Over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Test Conditions		Min	Typ	Max	Unit
V_{IK}	Input clamp voltage	I_I = -18 mA, V_{EN} = 0 V				-1.2	V
I_{IH}	Input leakage current	V_I = 5 V, V_{EN} = 0 V			0.5	5	μA
I_{CC}	Supply current	V_{REF_B} = V_{EN} = 5.5 V, V_{REF_A} = 4.5 V, I_O = 0 , V_I = V_{CC} or GND			0.05	±5	μA
$C_{I(EN)}$	Input capacitance	V_I = 3 V or 0 V			40		pF
$C_{IO(OFF)}$	Off capacitance	V_O = 3 V or 0 V, V_{EN} = 0 V			4	6	pF
$C_{IO(ON)}$	On capacitance	V_O = 3 V or 0 V, V_{EN} = 3V			10.5	12.5	pF
R_{ON} (Note 2)	On-state resistance	V_I = 0 V, V_{REF_B} = V_{EN} = 5 V, I_O = 64 mA	V_{REF_A} = 3.3 V		3		Ω
			V_{REF_A} = 2.5 V		3		
			V_{REF_A} = 1.8 V		4		
		V_I = 0 V, V_{REF_B} = V_{EN} = 5 V, I_O = 32 mA	V_{REF_A} = 3.3 V		3		Ω
			V_{REF_A} = 2.5 V		3		
			V_{REF_A} = 1.8 V		4		
			V_{REF_A} = 1 V		6		
		V_I = 1.8 V, V_{REF_B} = V_{EN} = 5 V I_O = 15 mA	V_{REF_A} = 3.3 V		4.5		Ω
		V_I = 1 V, V_{REF_B} = V_{EN} = 3.3 V I_O = 10 mA	V_{REF_A} = 1.8 V		7.5		Ω
		V_I = 0 V, V_{REF_B} = V_{EN} = 3.3 V I_O = 10 mA	V_{REF_A} = 1.0 V		6		Ω
		V_I = 0 V, V_{REF_B} = V_{EN} = 1.8 V I_O = 10 mA	V_{REF_A} = 1.0 V		6.5		Ω

Note 1: All typical values are at T_A = 25°C.

Note 2: Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.5 Switching Characteristics: Translating Down

Over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8-1).

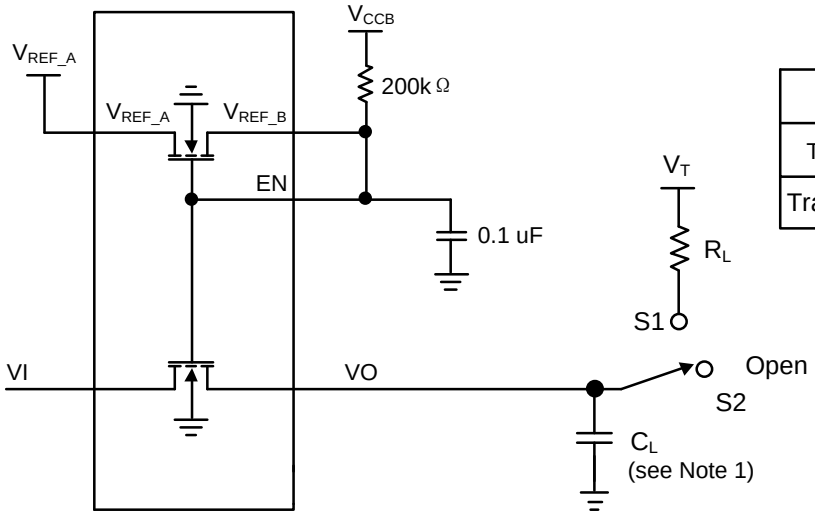
Parameter		Test conditions		Min	Typ	Max	Unit
t_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, V_{CCB} = V_{IH} = V_{REF_A} + 1V, V_{IL} = 0, V_M = 0.5V_{REF_A}	C_L=15pF		0.75		ns
			C_L=30pF		1.4		
			C_L=50pF		1.9		
t_{PHL}	High to low propagation delay		C_L=15pF		0.85		ns
			C_L=30pF		1.5		
			C_L=50pF		2		
t_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, V_{CCB} = V_{IH} = V_{REF_A} + 1V, V_{IL} = 0, V_M = 0.5V_{REF_A}	C_L=15pF		0.8		ns
			C_L=30pF		1.45		
			C_L=50pF		2		
t_{PHL}	High to low propagation delay		C_L=15pF		0.9		ns
			C_L=30pF		1.55		
			C_L=50pF		2.1		

7.6 Switching Characteristics (continued): Translating Up

Over recommended operating free-air temperature range (unless otherwise noted) (see Figure 8-1).

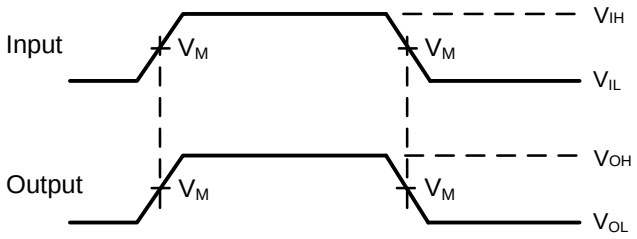
Parameter		Test conditions		Min	Typ	Max	Unit
t_{PLH}	Low-to-high propagation delay	V_{CCB} = 3.3 V, V_{CCB} = V_T = V_{REF_A} + 1V, V_{REF_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{REF_A} and R_L = 300 Ω	C_L=15pF		0.9		ns
			C_L=30pF		1.55		
			C_L=50pF		2.1		
t_{PHL}	High to low propagation delay		C_L=15pF		1		ns
			C_L=30pF		1.65		
			C_L=50pF		2.2		
t_{PLH}	Low-to-high propagation delay	V_{CCB} = 2.5 V, V_{CCB} = V_T = V_{REF_A} + 1V, V_{REF_A} = V_{IH}, V_{IL} = 0, V_M = 0.5V_{REF_A} and R_L = 300 Ω	C_L=15pF		0.8		ns
			C_L=30pF		1.35		
			C_L=50pF		1.8		
t_{PHL}	High to low propagation delay		C_L=15pF		0.9		ns
			C_L=30pF		1.45		
			C_L=50pF		1.9		

8 Parameter Measurement Information



Stage	Switch
Translating up	S1
Translating down	S2

a. Test circuit



b. Timing diagram

Note 1: C_L includes probe and jig capacitance.
Note 2: All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2 ns, t_F ≤ 2 ns.
Note 3: The outputs are measured one at a time, with one transition per measurement.

Figure 8-1. Waveforms and test circuit

9 Detailed Description

9.1 Overview

The UMLSF0108 can be used in level translation applications for interfacing devices or systems operating at different interface voltages without direction control pin. The devices are ideal for use in applications where an open-drain driver is connected to the data I/Os. The devices can achieve 100 MHz with the appropriate pull-up resistors and layout. What's more, the UMLSF0108 can also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram

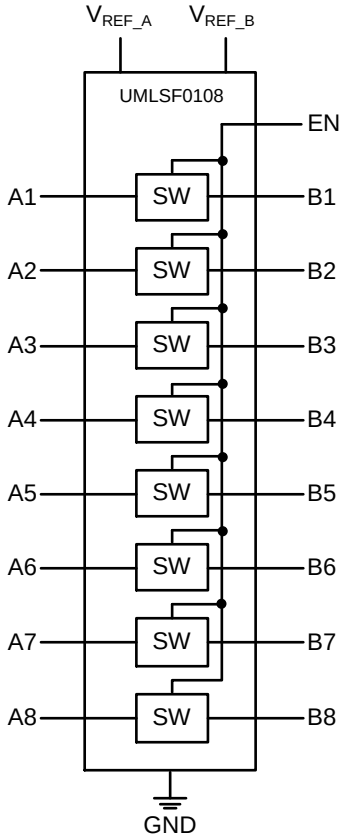


Figure 9-1. UMLSF0108 Block Diagram

10 Feature Description

10.1 Auto Bidirectional Voltage Translation

The device is an auto bidirectional voltage level translator that is operational from 0.8 to 4.5V on V_{REF_A} and 1.65 to 5.5V on V_{REF_B}. This allows bidirectional voltage translation between 0.8V and 5.5V without the need for a direction pin in open-drain or push-pull applications. The LSF family supports level translation applications with transmission speeds greater than 100 Mbps for open-drain systems using a 30-pF capacitance and 250-Ω pull-up resistor. Both the output driver of the controller and the peripheral device output can be push-pull or open-drain (pull-up resistors may be required). In both up and down translation, the B-side is often referred to as the high side and refers to devices connected to the B ports. The A-side can be referred to as the low side.

10.2 Output Enable

To enable the I/O pins, the EN input should be tied directly to V_{REF_B} during operation and both pins must be pulled up to the HIGH side (V_{CCB}) through a bias resistor (typically 200kΩ). To be in the high impedance state during power-up, power-down, or during operation, the EN pin must be LOW. The EN pin should always be tied directly to the V_{REF_B} pin and is recommended to be disabled by an open-drain driver without a pull-up resistor. This allows V_{REF_B} to regulate the EN input and bias the channels for proper translation. A filter capacitor on V_{REF_B} is recommended for a stable supply at the device.
The supply voltage of open drain I/O devices can be completely different from the supplies used for the LSF and has no impact on the operation.

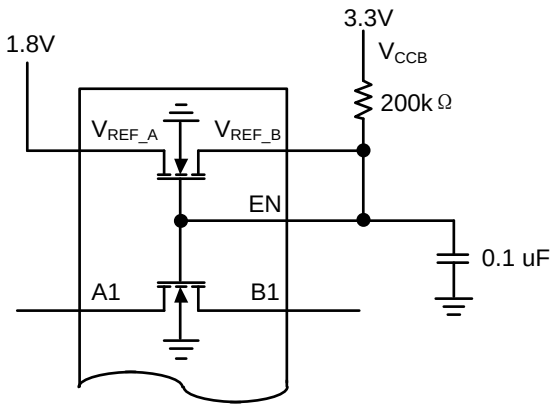


Figure 10-1. Enable Pin Tied to V_{REF_B} Directly and to V_{CCB} Through a Bias Resistor

Table 10-1. Enable Pin Function Table

Input EN Pin	Function
Tied directly to V_{REF_B}	An = Bn
L	Hi-Z

10.3 Device Functional Modes

For each channel (n), when either the An or Bn port is LOW, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled LOW. The low RON of the switch allows connections to be made with minimal propagation delay and signal distortion.

10.3 Device Functional Modes (continued)

Table 10-2. UMLSF0108 Functionality

Signal Direction (Note 1)	Input State	Switch State	Function
B to A (Down Translation)	B = LOW	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage.
	B = HIGH	OFF (High Impedance)	A-side voltage is clamped at V_{REF_A}. (Note 2)
A to B (Up Translation)	A = LOW	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage.
	A = HIGH	OFF (High Impedance)	B-side voltage is clamped at V_{REF_A} and then pulled up to the V_{PU} supply voltage.

Note 1: The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
Note 2: The A-side can have a pull-up to V_{REF_A} for additional current drive capability or may also be pulled above V_{REF_A} with a pull-up resistor.

10.3.1 Up and Down Translation

10.3.1.1 Up Translation

When the signal is being driven from A to B and the An port is HIGH, the switch will be OFF and the Bn port will then be driven to a voltage higher than V_{REF_A} by the pull-up resistor that is connected to the pull-up supply voltage (V_{PU}). This functionality allows seamless translation between higher and lower voltages selected by the user, without the need for directional control.

Up translation with the UMLSF0108 requires attention to two important factors: maximum data rate and sink current. Maximum data rate is directly related to the rising edge of the output signal. Sink current depends on supply values and the chosen pull-up resistor values. And a low RC value is needed to reach high speeds, which also require strong drivers.

10.3.1.2 Down Translation

When the signal is being driven HIGH from the Bn port to An port, the switch will be OFF, clamping the voltage on the An port to the voltage set by V_{REF_A}. A pull-up resistor can be added on either side of the device. There are special circumstances that allow the removal of one or both of the pull-up resistors. If the signal is always going to be down translated from a push-pull transmitter, then the resistor on the B-side can be removed. If the leakage current into the receiver on the A-side is less than 1μA, then the resistor on the A-side can also be removed. This arrangement with no external pull-up resistors can be used when down translating from a push-pull output to a low-leakage input. For an open drain transmitter, the pull-up resistor on the B-side is necessary because an open drain output can't drive high by itself.

11 Application Information

11.1 Application Information

The UMLSF0108 is suitable for open-drain or push-pull interface like GPIO, SPI. MDIO, SMBus, PMBus, I²C, UART, SVID.

11.2 Typical Application

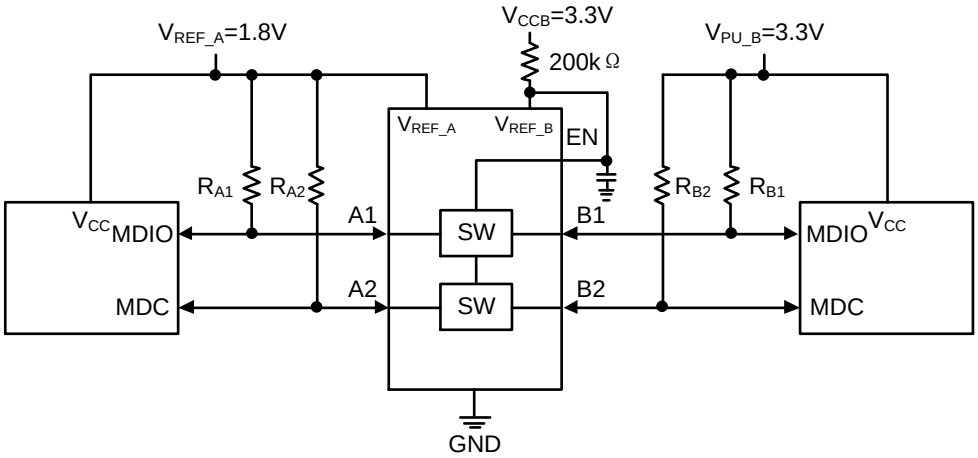
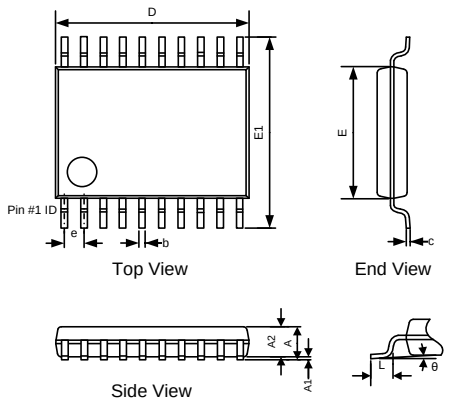


Figure 11-1. UMLSF0108 MDIO Bidirectional Translation

Package Information

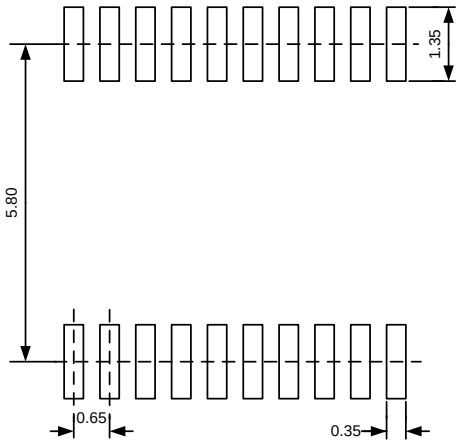
TSSOP20

Outline Drawing



Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	-	1.05	0.031	-	0.041
b	0.19	-	0.30	0.007	-	0.012
c	0.09	-	0.20	0.004	-	0.008
D	6.40	6.50	6.60	0.252	0.256	0.260
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	-	0.75	0.018	-	0.030
θ	0°	-	8°	0°	-	8°

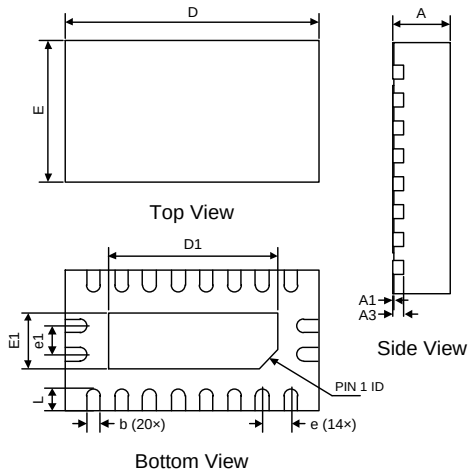
Land Pattern



NOTES:
1. Unit: mm.
2. General tolerance ±0.05mm unless otherwise specified.
3. The layout is just for reference.

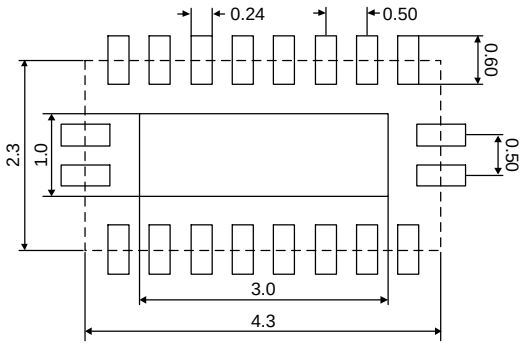
QFN20 4.5×2.5

Outline Drawing



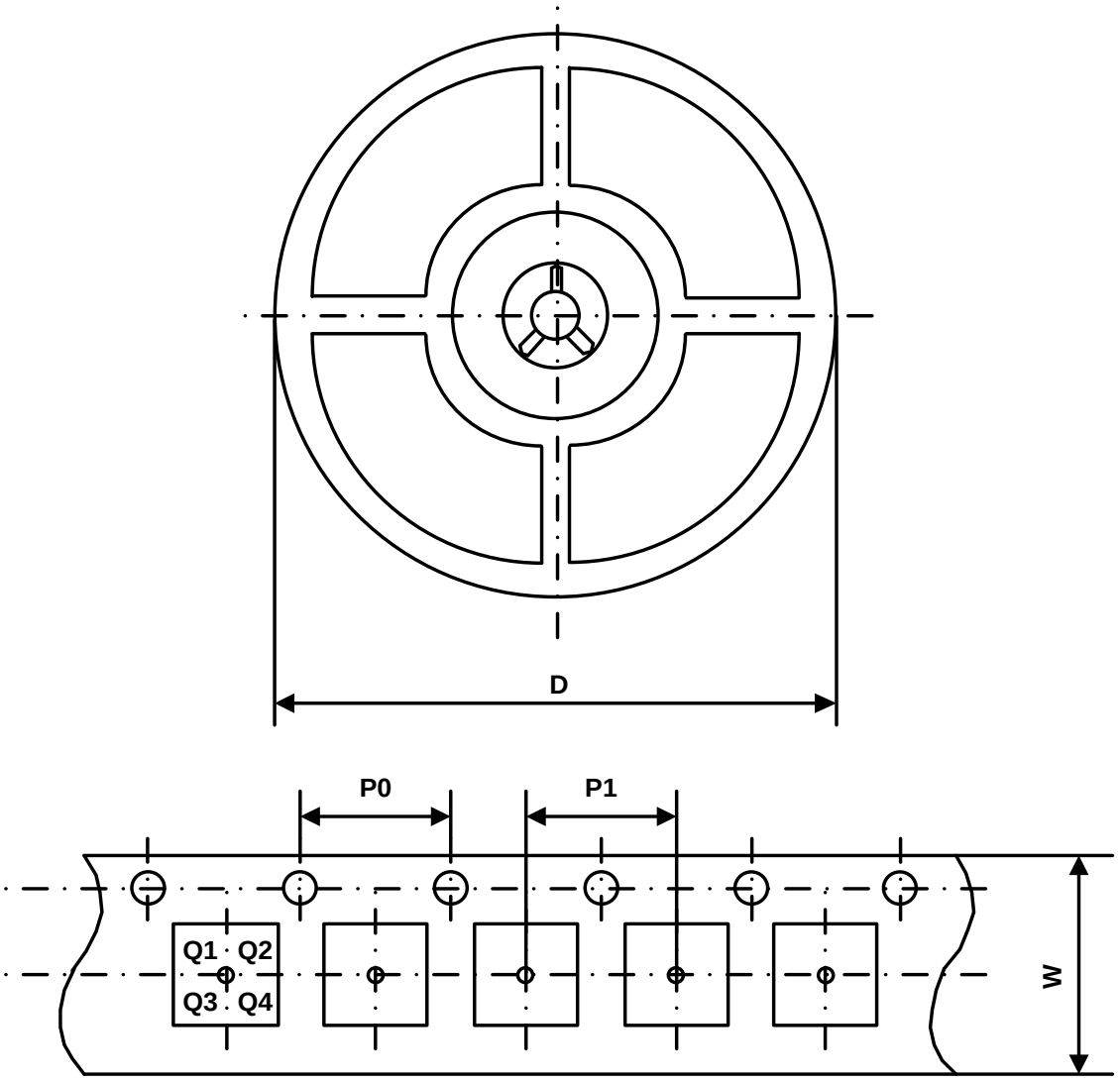
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.70	-	1.00	0.028	-	0.040
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20TYP			0.008TYP		
b	0.18	-	0.30	0.008	-	0.012
D	4.40	4.50	4.60	0.176	0.180	0.184
D1	2.70	-	3.20	0.108	-	0.128
E	2.40	2.50	2.60	0.096	0.100	0.104
E1	0.70	-	1.20	0.028	-	0.048
e	0.50BSC			0.020BSC		
e1	0.50BSC			0.020BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Land Pattern



NOTES:
1. Unit: mm.
2. General tolerance ±0.05mm unless otherwise specified.
3. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMLSF0108UK	TSSOP20	16 mm	4 mm	12 mm	330 mm	Q1
UMLSF0108QCK	QFN20 4.5×2.5	12 mm	4 mm	8 mm	330 mm	Q1

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