2-Bit Ultra-Small Bidirectional Multi-Voltage Level Translator for Open-Drain and Push-Pull Application

UMLSF0002DE6 ***DFN6 1.0×0.8***

1 Description

The UMLSF0002 allows for bidirectional voltage translations between 0.8 V and 5.0 V without the need for a direction terminal in open-drain or push-pull applications. The device supports up to 100MHz up translation and greater than 100MHz down translation at ≤ 30pF capacitive load and up to 40MHz up or down translation at 50pF capacitive load.

The UMLSF0002 supports 5V tolerance on I/O port. The ability to set up different voltage translation levels on each channel makes it very flexible in industrial and telecom applications.

The UMLSF0002 replace the VREF_A, VREF_B power supplies and the 200kΩ bias resistor with the VBIAS pin. The UMLSF0002 utilizes the VBIAS pin that enables translation by being biased to the same voltage as the lower power supply at the I/Os that is being translated to and from.

The UMLSF0002 is available in DFN6 1.0×0.8 package.

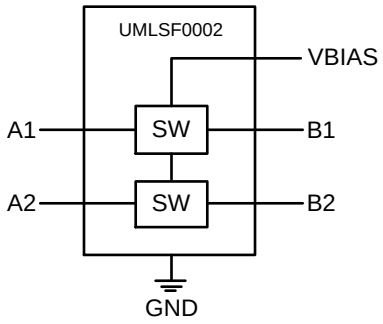
2 Features

- Bidirectional voltage translation with no direction pin
- Allow bidirectional voltage level translation between:
  - 0.8 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.2 V ↔ 1.8, 2.5, 3.3, 5 V
  - 1.8 V ↔ 2.5, 3.3, 5 V
  - 2.5 V ↔ 3.3, 5 V
  - 3.3 V ↔ 5 V
- ESD protection
  - ±4000V Human body model
  - ±2000V Charged-device model
- Up translation
  - ≤ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≤ 40MHz (80Mbps); C_L = 50 pF
- Down translation
  - ≥ 100MHz (200Mbps); C_L ≤ 30 pF
  - ≥ 40MHz (80Mbps); C_L = 50 pF
- Low standby current
- 5 V Tolerance I/O port to support TTL
- Low R_{ON} provides less signal distortion
- High-impedance I/O terminals when V_{BIAS} = 0V
- Latch-up performance exceeds 200 mA per JESD 78

3 Applications

- GPIO, MDIO, PMBus, SMBus, SDIO, UART, I^2C and other interfaces in telecom infrastructure
- Personal computing
- Industrial
- Automotive

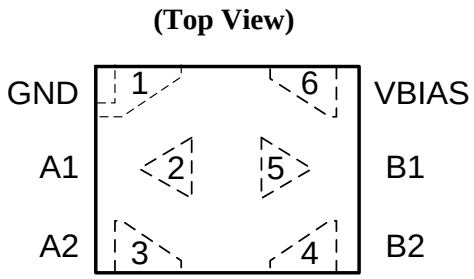
4 Simplified Schematic

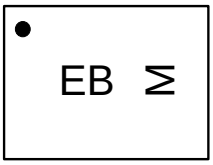


5 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UMLSF0002DE6	EB	DFN6 1.0×0.8	10000pcs/7Inch Tape & Reel

6 Pin Configuration and Function





M: Month Code
UMLSF0002DE6
DFN6 1.0×0.8

Table 6-1. Pin Functions

Pin No.	Pin Name	Function
1	GND	Ground.
2	A1	Input/output A1.
3	A2	Input/output A2.
4	B2	Input/output B2.
5	B1	Input/output B1.
6	VBIAS	Enable input / Supply Voltage.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter		Value	Unit
V_I	Input Voltage (Note 2)		-0.5 to +7	V
$V_{I/O}$	Input/output voltage (Note 2)		-0.5 to +7	V
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001		±4000	V
	Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002		±2000	V
	Continuous channel current		128	mA
I_{IK}	Input clamp current	$V_I < 0$	-50	mA
T_J	Operating Junction Temperature		-40 to +150	℃
T_{STG}	Storage Temperature		-65 to +150	℃

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: The input and input/output negative-voltage ratings may be exceeded if the input and input/output clamp-current ratings are observed.

7.2 Recommended Operating Conditions

Over recommended operating free-air temperature range (unless otherwise noted).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	Input/output voltage	A1, A2, B1, B2	0	5.5	V
V_{BIAS}	Reference voltage		0	5.5	V
I_{PASS}	Pass transistor current			64	mA
T_A	Operating free-air temperature		-40	125	℃

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction-to-ambient thermal resistance	DFN6 1.0×0.8	294.4	℃/W
$R_{\theta JC(TOP)}$	Junction-to-case (top) thermal resistance	DFN6 1.0×0.8	188.9	℃/W
$R_{\theta JB}$	Junction-to-board thermal resistance	DFN6 1.0×0.8	216.8	℃/W

7.4 Electrical Characteristics (Note 1)

Over recommended operating free-air temperature range (unless otherwise noted).

Parameter		Test Conditions		Min	Typ	Max	Unit
V_{IK}		I_I = -18 mA, V_{BIAS} = 0 V				-1.2	V
I_{IH}		V_I = 5 V, V_{BIAS} = 0 V				5	μA
$C_{I(BIAS)}$		V_I = 3 V or 0 V			11		pF
$C_{IO(OFF)}$		V_O = 3 V or 0 V, V_{BIAS} = 0 V			4	6	pF
$C_{IO(ON)}$		V_O = 3 V or 0 V, V_{BIAS} = 3V			10.5	12.5	pF
R_{ON} (Note 2)	ON-State Resistance	V_I=0; I_O=64mA	V_{BIAS} =4.5V		2.8		Ω
			V_{BIAS} =3V		3.8		
			V_{BIAS} =2.3V		5.1		
		V_I=0; I_O=32mA	V_{BIAS} =1.5V		12		
		V_I=2.4V; I_O=15mA	V_{BIAS} =4.5V		8		
			V_{BIAS} =3V		68		
		V_I=1.7V; I_O=15mA	V_{BIAS} =2.3V		58		

Note 1: All typical values are at T_A = 25°C.

Note 2: Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

7.5 Switching Characteristics (Translating Down)

Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

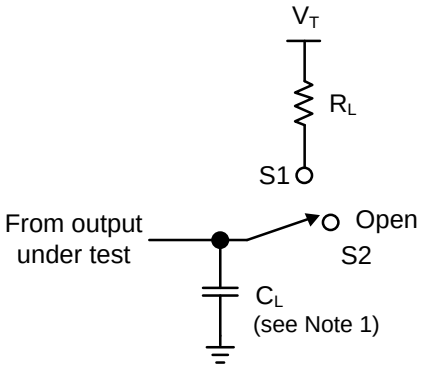
Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
V_{BIAS} = 2.3V; V_{IH} = 3.3V; V_{IL} = 0V; V_M =1.15V(see Figure 8-1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) A or B to (Output) B or A	1.9		1.4		0.75		ns
t_{PHL}	HIGH to LOW Propagation Delay		2		1.5		0.85		ns
V_{BIAS} =1.5V; V_{IH} = 2.5V; V_{IL} = 0V; V_M = 0.75V (see Figure 8-1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) A or B to (Output) B or A	2		1.45		0.8		ns
t_{PHL}	HIGH to LOW Propagation Delay		2.1		1.55		0.9		ns

7.6 Switching Characteristics (Translating Up)

Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

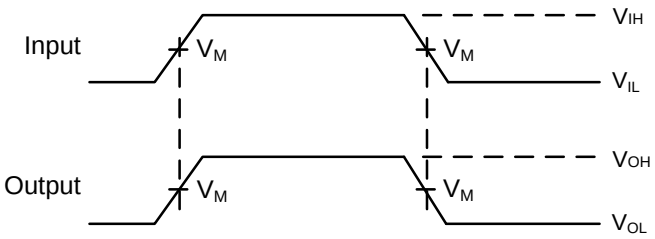
Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Typ	Max	Typ	Max	Typ	Max	
V_{BIAS} = 2.3V; V_{IH} = 2.3V; V_{IL} = 0V; V_T = 3.3V; V_M =1.15V ; R_L =300 Ω (see Figure 8-1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) A or B to (Output) B or A	2.1		1.55		0.9		ns
t_{PHL}	HIGH to LOW Propagation Delay		2.2		1.65		1		ns
V_{BIAS} =1.5V; V_{IH} = 1.5V; V_{IL} = 0V; V_T = 2.5V; V_M = 0.75V ; R_L =300 Ω (see Figure 8-1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) A or B to (Output) B or A	1.8		1.35		0.8		ns
t_{PHL}	HIGH to LOW Propagation Delay		1.9		1.45		0.9		ns

8 Parameter Measurement Information



Load circuit

Stage	Switch
Translating up	S1
Translating down	S2



Timing diagram; high-impedance scope probe used

Note 1: C_L includes probe and jig capacitance.
Note 2: All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50Ω, t_R ≤ 2 ns, t_F ≤ 2 ns.
Note 3: The outputs are measured one at a time, with one transition per measurement.

Figure 8-1. Load Circuit for Outputs

9 Detailed Description

9.1 Overview

The UMLSF0002 may be used in level translation applications for interfacing devices or systems operating with one another that operate at different interface voltages as well as for switching applications where V_{EXT_A} = V_{EXT_B}. The device is ideal for use in applications where an open-drain driver is connected to the data I/Os. The device can achieve 100 MHz with the appropriate pull-up resistors and layout. What's more, the UMLSF0002 may also be used in applications where a push-pull driver is connected to the data I/Os.

9.2 Functional Block Diagram

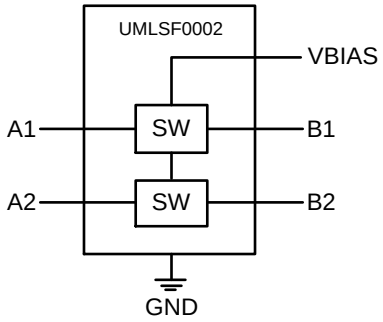


Figure 9-1. UMLSF0002 Block Diagram

10 Feature Description

10.1 Support High Speed Translation, Greater than 100MHz

The UMLSF0002 supports more consumer or telecom interfaces (MDIO or SDIO).

10.2 Bidirectional Voltage Translation Without DIR Terminal

The UMLSF0002 supports automatic direction voltage translation that minimizes system effort to develop voltage translation for bidirectional interface (PMBus, I^2C, or SMbus).

10.3 5V Tolerance on IO Port and 125°C Support

The UMLSF0002 features 5V tolerance and -40°C to 125°C operating temperature range that compliant with TTL levels in industrial and telecom applications.

10.4 V_{BIAS}/Enable

To enable the I/O pins, the V_{BIAS} input should be referenced towards the lower power supply between V_{EXT_A} and V_{EXT_B} (in the following example, V_{EXT_A}) during voltage translation. To ensure the device to be in the high impedance state during power-up, power-down, or during operation, the V_{BIAS} pin must be pulled low and at GND or disabled by an open-drain driver without a pull-up resistor. Use the V_{BIAS} pin to properly bias the I/O channels. Placing a filter capacitor on V_{BIAS} closely is also recommended for a stable supply at the device.

10.4 V_{BIAS}/Enable (continued)

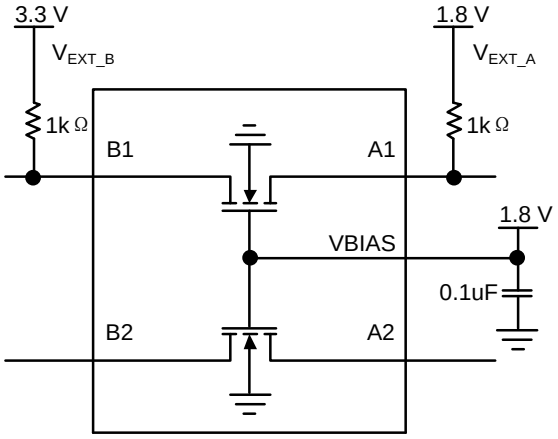


Table 10-1. V_{BIAS} tied to Lower Power Supply

Input V_{BIAS} terminal	Function
Tied to Lower Power Supply	An, Bn channel Enabled
L	Hi-Z

10.5 Functional Modes

For each channel (n), when either the An or Bn port is Low, the switch provides a low impedance path between the An and Bn ports; the corresponding Bn or An port will be pulled Low. The low R_{ON} of the switch allows connections to be made with minimal propagation delay and signal distortion.
Table 10-2 lists the device functional modes of the UMLSF0002.

Table 10-2. Function Table (Note1, 2)

Signal Direction	Input State	Switch State	Function
B to A (Down Translation)	B = Low	ON (Low Impedance)	A-side voltage is pulled low through the switch to the B-side voltage
	B = High	Off (High Impedance)	A-side voltage is clamped at V_{EXT_A}
A to B (Up Translation)	A = Low	ON (Low Impedance)	B-side voltage is pulled low through the switch to the A-side voltage
	A = High	Off (High Impedance)	B-side voltage is clamped at V_{EXT_A} and then pulled up to the V_{EXT_B} supply voltage

Note 1: The downstream channel should not be actively driven through a low impedance driver, or else bus contention may occur.
Note 2: The A-side can have a pull-up to V_{EXT_A} for additional current drive capability or may also be pulled above V_{EXT_A} with a pull-up resistor.

11 Application Information

11.1 Application Information

The UMLSF0002 is suitable for open-drain or push-pull interface like GPIO, SPI. MDIO, SMBus, PMBus, I²C, UART, SVID.

11.2 Typical Applications

The UMLSF0002 series are suitable for open-drain or push-pull interface like GPIO, SPI. MDIO, SMBus, PMBus, I²C, UART, SVID.

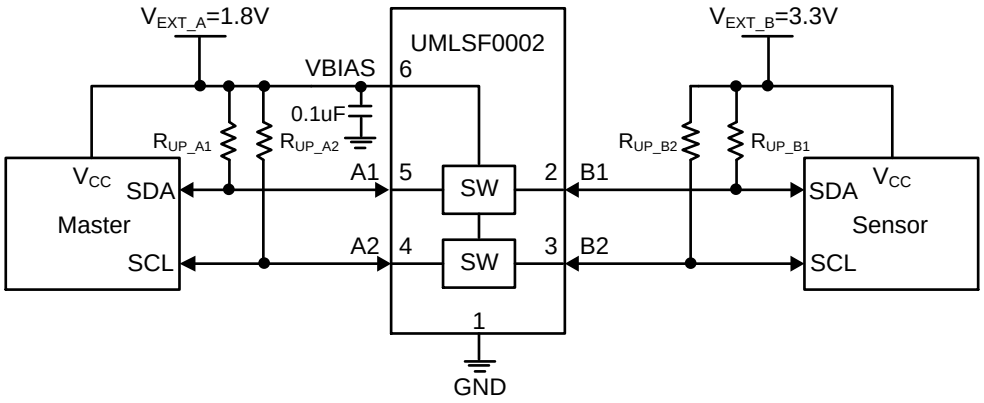
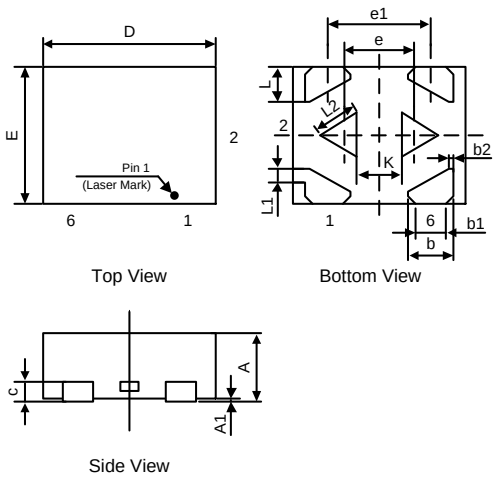


Figure 11-1. UMLSF0002 I²C Bidirectional Translation

Package Information

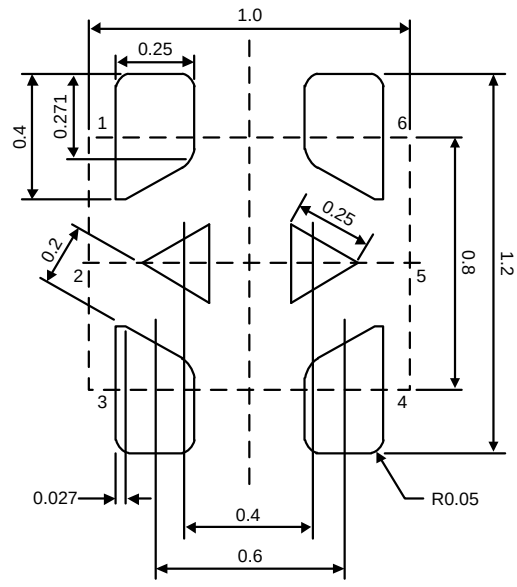
DFN6 1.0×0.8

Outline Drawing



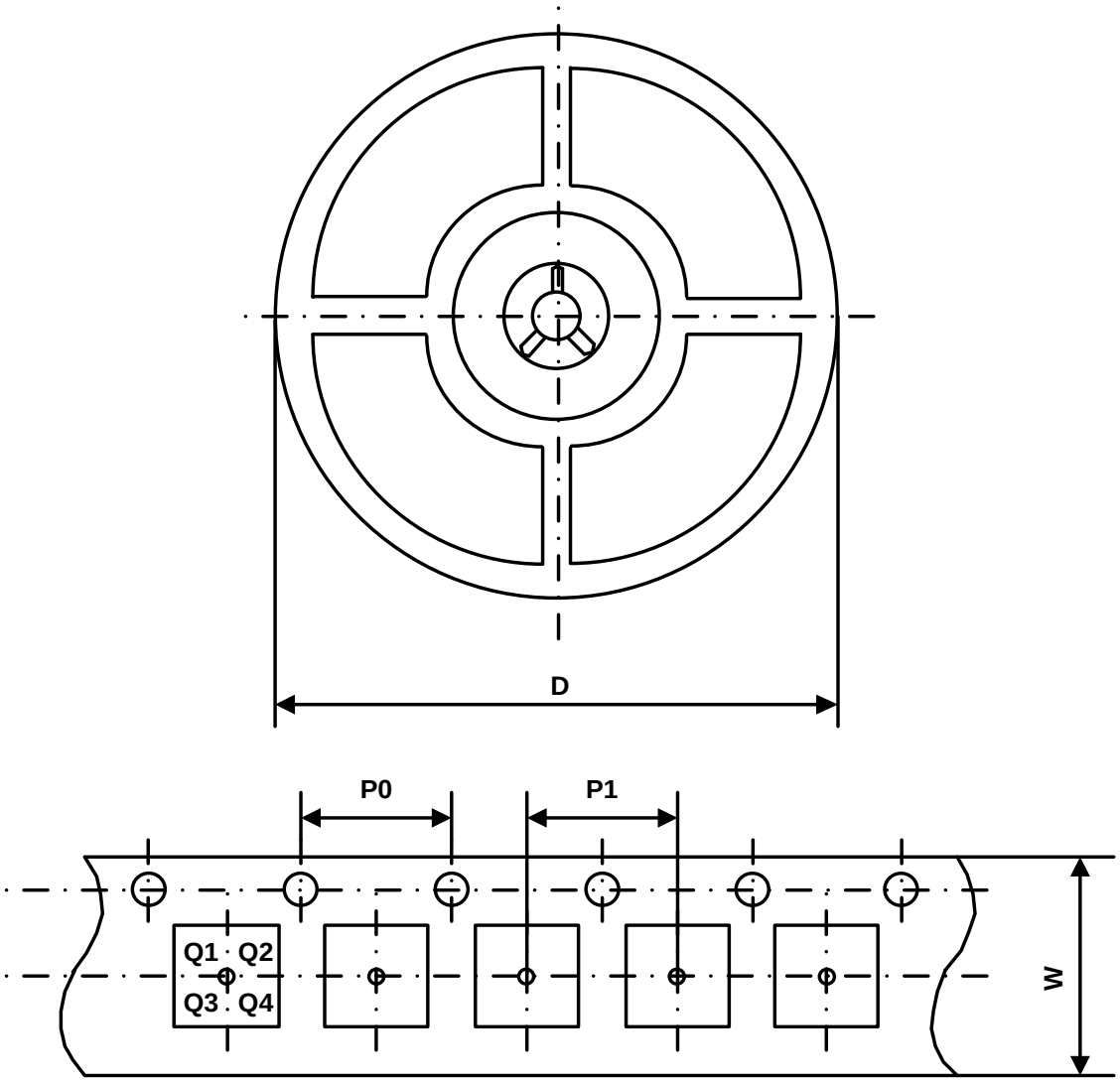
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.35	-	0.40	0.014	-	0.016
A1	0.00	-	0.05	0.000	0.001	0.002
b	0.21	0.26	0.31	0.008	0.010	0.012
b1	0.15REF			0.006REF		
b2	0.027REF			0.001REF		
c	0.127REF			0.005REF		
D	0.95	1.00	1.05	0.038	0.040	0.042
e	0.40BSC			0.016BSC		
e1	0.60BSC			0.024BSC		
E	0.75	0.80	0.85	0.030	0.032	0.034
L	0.16	0.21	0.26	0.006	0.008	0.010
L1	0.08REF			0.003REF		
L2	0.20	0.25	0.30	0.008	0.010	0.012
K	0.256REF			0.010REF		

Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMLSF0002DE	DFN6 1.0×0.8	8 mm	4 mm	2 mm	180 mm	Q2

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