High Speed, Isolated RS-485/RS-422 Transceivers

UMISO3481 *WSOP16/WSSOP10*
UMISO13082 *WSOP16/WSSOP10*
UMISO3481F *WSOP16*
UMISO13082F *WSOP16*

1 Description

The UMISO3481, UMISO13082, UMISO3481F and UMISO13082F are galvanically-isolated differential line transceivers for TIA/EIA RS-485 and RS-422 applications. Both devices support 5000 V_{RMS} insulation withstand voltages, while providing high electromagnetic immunity and low emissions at low power consumption.

The devices are available in two speed grades. The UMISO3481 and UMISO3481F are available in 1Mbps. The UMISO13082 and UMISO13082F are available in 20Mbps. Any cabled I/O can be subjected to electrical noise transients from various sources. The devices' bus pins can endure high levels of IEC electrostatic discharge (ESD) and IEC electrical fast transient (EFT) events. These isolated devices can significantly increase protection and reduce the risk of damage to expensive control circuits.

The UMISO3481 and UMISO13082 are available in WSSOP10 and WSOP16 packages. The UMISO3481F and UMISO13082F are available in WSOP16 package. All devices are characterized over ambient free-air temperatures from -40°C to 125°C.

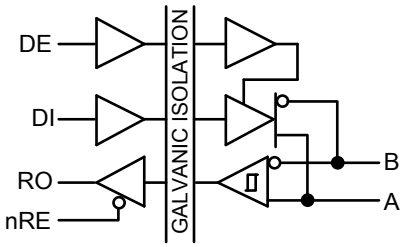
2 Features

- Compatible with the requirements of the TIA/EIA-485A standards
- Differential output exceeds 2.1 V for PROFIBUS compatibility with 5V supply
- 3V to 5.5V logic-side supply (V_{CCA}), 3V to 5.5V bus-side supply (V_{CCB})
- Integrated protection increases robustness
  - Up to 5000 V_{RMS} isolation rating
  - ±200 kV/μs typical CMTI
  - Bus fault protection of ±18V
- Half/Full duplex device available in two speed grades:
  - 1Mbps (UMISO3481,UMISO3481F)
  - 20Mbps (UMISO13082,UMISO13082F)
- Extended ambient temperature range: -40°C to 125°C
- Glitch-free power-up and power-down for hot plugin
- Open, short, and idle bus failsafe
- Thermal shutdown
- 1/8 unit load (up to 256 bus nodes)
- WSSOP10 and WSOP16 package
- Compliant with safety regulatory
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL according to UL1577
  - IEC 61010-1 and GB 4943.1-2022

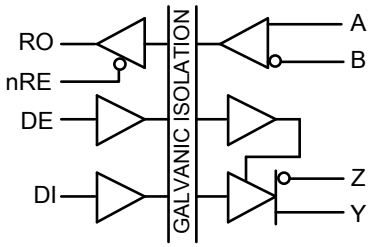
3 Applications

- Grid infrastructure
- Solar inverter
- Factory automation & control
- Motor drives
- HVAC systems and building automation
- Networked security stations

4 Functional Diagram



UMISO3481, UMISO13082 Function Diagram

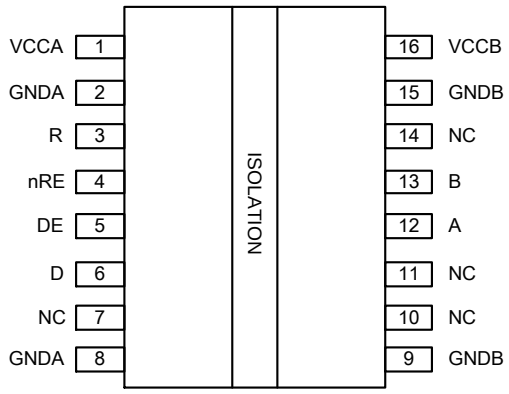


UMISO3481F, UMISO13082F Function Diagram

5 Ordering Information

Part Number	Duplex	Mark Code	Isolation Rating (V_{RMS})	Package Type	Shipping Qty
UMISO3481WAB	Half	UMISO3481	5000	WSSOP10	4000pcs/13Inch Tape & Reel
UMISO3481WSG	Half	UMISO3481	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO13082WAB	Half	UMISO13082	5000	WSSOP10	4000pcs/13Inch Tape & Reel
UMISO13082WSG	Half	UMISO13082	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO3481FWSG	Full	UMISO3481F	5000	WSOP16	1500pcs/13Inch Tape & Reel
UMISO13082FWSG	Full	UMISO13082F	5000	WSOP16	1500pcs/13Inch Tape & Reel

6 Pin Configuration and Function

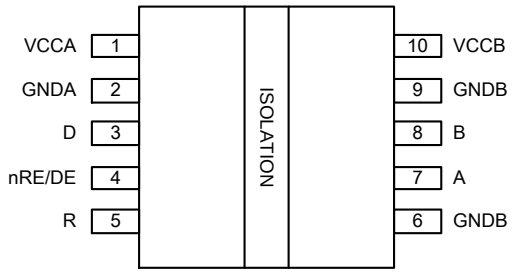


UMISO3481 / UMISO13082
WSOP16

Table 6-1. Pin Functions of WSOP16 package for UMISO3481 and UMISO13082

Pin No.	Pin Name	Function
1	VCCA	Logic-side power supply.
2, 8	GNDA	Ground connection for VCCA.
3	R	Receiver output.
4	nRE	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
5	DE	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
6	D	Driver input.
9, 15	GNDB	Ground connection for VCCB.
7, 10, 11, 14	NC	Not connected internally. Can be connected to supply, ground or left open on PCB.
12	A	Transceiver non-inverting input or output (I/O) on the bus side.
13	B	Transceiver inverting input or output (I/O) on the bus side.
16	VCCB	Transceiver-side power supply.

6 Pin Configuration and Function (continued)

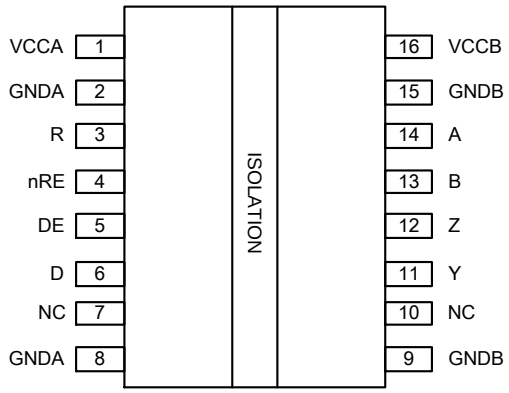


UMISO3481 / UMISO13082
WSSOP10

Table 6-2. Pin Functions of WSSOP10 package for UMISO3481 and UMISO13082

Pin No.	Pin Name	Function
1	VCCA	Logic-side power supply.
2	GNDA	Ground connection for VCCA.
3	D	Driver input.
4	nRE/DE	Driver or Receiver select. High = Driver enable and Receiver disable, Low = Receiver enable and Driver disable. Connect this pin to ground with a 100kΩ resistor to avoid floating.
5	R	Receiver output.
6, 9	GNDB	Ground connection for VCCB.
7	A	Transceiver non-inverting input or output (I/O) on the bus side.
8	B	Transceiver inverting input or output (I/O) on the bus side.
10	VCCB	Transceiver-side power supply.

6 Pin Configuration and Function (continued)



UMISO3481F / UMISO13082F
WSOP16

Table 6-3. Pin Functions of WSOP16 package for UMISO3481F and UMISO13082F

Pin No.	Pin Name	Function
1	VCCA	Logic-side power supply.
2, 8	GNDA	Ground connection for VCCA.
3	R	Receiver output.
4	nRE	Receiver enable. This pin disables the receiver output when high or open and enables the receiver output when low.
5	DE	Driver enable. This pin enables the driver output when high and disables the driver output when low or open.
6	D	Driver input.
9, 15	GNDB	Ground connection for VCCB.
7, 10	NC	Not connected internally. Can be connected to supply, ground or left open on PCB.
11	Y	Driver non-inverting output.
12	Z	Driver inverting output.
13	B	Receiver inverting input on the bus side.
14	A	Receiver non-inverting input on the bus side.
16	VCCB	Transceiver-side power supply.

7 Specifications

7.1 Absolute Maximum Ratings (Note 1, 2)

Symbol	Parameter		Min	Typ	Max	Uni
V_{CCA}, V_{CCB}	Supply voltage		-0.5		6.5	V
V_{IO}	Voltage on A, B, Y, Z		-18		18	V
	Voltage on any logic pin (D, DE, nRE, R, nRE/DE) (Note 3)		-0.5		V_{CCA} +0.5	V
I_O	Output current on R pin		-24		24	mA
T_{STG}	Storage temperature		-65		150	℃
T_J	Junction temperature		-40		150	℃
V_{ESD}	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001	Logic-Side All Pins to GNDA		±8		kV
		Bus-Side All Pins to GNDB		±8		kV
I_{LU}	Latch up, per JEDEC JESD78			±200		mA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GNDA or GNDB) and are peak voltage values.
Note 3: Maximum voltage must not exceed 6.5 V.

7.2 Recommended Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
V_{CCA}	Supply Voltage		3	3.3/5	5.5	V
V_{CCB}	Supply Voltage		3	3.3/5	5.5	V
V_I	Input voltage at any bus terminal (separately or common mode)		-15		15	V
V_{ID}	Differential input voltage		-15		15	V
I_O	Output current, driver		-60		60	mA
I_{OR}	Output current, receiver		-8		8	mA
R_L	Differential load resistance		54	60		Ω
1/ t_{UI}	Signaling rate	UMISO3481, UMISO3481F			1	Mbps
		UMISO13082, UMISO13082F			20	Mbps
T_A	Operating ambient temperature		-40		125	℃

7.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	WSOP16	82	°C/W
		WSSOP10	99	°C/W

7.4 Insulation Specifications

Symbol	Parameter	Conditions	Value		Unit
			WSOP16	WSSOP10	
CLR	External clearance	Shortest terminal-to-terminal distance through air	8	8	mm
CPG	External creepage	Shortest terminal-to-terminal distance across the package surface	8	8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	>20	>20	μm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	>600	>600	V
	Material group	Per IEC 60664-1	I	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 150 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 300 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-II	I-II	
DIN V VDE V 0884-17:2021-10 (Note 1)					
V_{IORM}	Maximum repetitive peak isolation voltage	AC voltage (bipolar)	1414	1414	V_{PK}
V_{IOWM}	Maximum operating isolation voltage	AC voltage; time-dependent dielectric breakdown (TDDB) test	1000	1000	V_{RMS}
		DC voltage	1414	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (certified); $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% product test)	7070	7070	V_{PK}
V_{IMP}	Maximum impulse voltage	Tested in air, 1.2/50 μs waveform per IEC 62368-1,	7500	7500	V_{PK}
V_{IOSM}	Maximum surge isolation voltage	$V_{IOSM} \geq 1.3 \times V_{IMP}$; Tested in oil (qualification test), 1.2/50 μs waveform per IEC 62368-1	10000	10000	V_{PK}

7.4 Insulation Specifications (Continued)

Symbol	Parameter	Conditions	Value		Unit
			WSOP16	WSSOP10	
q_{pd}	Apparent charge (Note 2)	Method a, after input/output safety test of the subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s	≤5	≤5	pC
		Method a, after environmental test of the subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.3 × V_{IORM}, t_m = 10 s	≤5	≤5	pC
		Method b, at routine test (100% production test) and preconditioning (type test) V_{ini} = 1.2 × V_{IOTM}, t_{ini} = 1 s; $V_{pd(m)}$ = 1.875 × V_{IORM} (for reinforced devices) or $V_{pd(m)}$ = 1.5 × V_{IORM} (for basic devices), t_m = 1 s (method b1) or $V_{pd(m)}$ = V_{ini}, t_m = t_{ini} (method b2)	≤5	≤5	pC
C_{IO}	Barrier capacitance, input to output (Note 3)	V_{IO} = 0.4 × sin (2πft), f = 1 MHz	1.0	1.0	pF
R_{IO}	Isolation resistance (Note 3)	V_{IO} = 500 V, T_A = 25 ℃	$>10^{12}$	$>10^{12}$	Ω
		V_{IO} = 500 V, 100 ℃ ≤ T_A ≤ 125 ℃	$>10^{11}$	$>10^{11}$	
		V_{IO} = 500 V at T_S = 150 ℃	$>10^{9}$	$>10^{9}$	
	Pollution degree		2	2	
UL 1577					
V_{ISO}	Maximum withstanding isolation voltage	V_{TEST} = V_{ISO}, t = 60s (qualification) V_{TEST} = 1.2 × V_{ISO}, t = 1 s (100% production test)	5000	5000	V_{RMS}

Note 1: This coupler is suitable for "safe electrical insulation" only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
Note 2: The characterization charge is discharging charge (pd) caused by partial discharge.
Note 3: Capacitance and resistance are measured with all pins on field-side and logic-side tied together.

7.5 Electrical Characteristics

V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V, T_A = -40°C to 125°C, unless otherwise noted. All typical values are at 25°C and supply voltage of V_{CCA} = 5 V, V_{CCB} = 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply						
I_{CCA}	Logic-side supply current	DE/nRE=V_{CCA} or 0 V, V_{CCA} = 3.3 V			7.6	mA
		DE/nRE=V_{CCA} or 0 V, V_{CCA} = 5 V			8	mA
I_{CCB}	Bus-side supply current	nRE = V_{CCA} or 0 V, DE = 0 V			6.8	mA
Driver						
$\|V_{OD}\|$	Driver differential output voltage magnitude	No load, V_{CCB} = 5 V	2.7	5	5.5	V
		R_L = 60 Ω, –15 V ≤ V_{TEST} ≤ 15V, 3V ≤ V_{CCB} ≤ 3.6V, See Figure 8-1	1.5	3.35		V
		R_L = 60 Ω, –15 V ≤ V_{TEST} ≤ 15V, 4.5 V ≤ V_{CCB} ≤ 5.5 V, See Figure 8-1	2.1	3.35		V
		R_L = 100 Ω, See Figure 8-2	2	4		V
		R_L = 54 Ω, See Figure 8-2	1.5	3.35		V
$\Delta\|V_{OD}\|$	Change in magnitude of driver differential output voltage	R_L= 54 Ω or 100 Ω See Figure 8-2	-150		150	mV
V_{OC}	Common-mode output voltage	R_L= 54 Ω or 100 Ω See Figure 8-2	1	V_{CCB}/2	3	V
$\Delta V_{OC(SS)}$	Steady-state common-mode output voltage	R_L= 54 Ω or 100 Ω See Figure 8-2	-100		100	mV
I_{OS}	Short-circuit output current	DE = V_{CCA}, -15V ≤ ($V_{A(Z)}$ or $V_{B(Y)}$) ≤ 15V	-250		250	mA
V_{IH}	Input High Voltage	DE, D	0.7V_{CCA}			V
V_{IL}	Input low Voltage	DE, D			0.3V_{CCA}	V
I_{I1}	Input current on DE pin or D pin	0 V ≤ V_{IN} ≤ V_{CCA}	-10		10	μA

7.5 Electrical Characteristics (continued)

V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V, T_A = -40°C to 125°C, unless otherwise noted. All typical values are at 25°C and supply voltage of V_{CCA} = 5 V, V_{CCB} = 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Receiver						
I_{I2}	Bus input current	DE = 0V, V_{CCB} = 0V or 5.5V, V_I =12V		70	125	μA
		DE = 0V, V_{CCB} = 0V or 5.5V, V_I =-7V	-100	-60		
V_{TH+}	Positive-going input threshold voltage	Over common-mode range of ±15 V		125	200	mV
V_{TH-}	Negative-going input threshold voltage		-200	-125		
V_{HYS}	Input hysteresis			250		
V_{OH}	Output high voltage	V_{CCA} = 5V I_{OH} = –4 mA	V_{CCA}-0.4	V_{CCA}-0.2		V
V_{OL}	Output low voltage	V_{CCA} = 5V I_{OH} = 4 mA		0.2	0.4	V
I_{OZ}	Output high-impedance current	V_O = 0 V or V_{CCA}, nRE = V_{CCA}	-10		10	μA
V_{IH}	Input High Voltage	nRE	0.7× V_{CCA}			V
V_{IL}	Input low Voltage	nRE			0.3× V_{CCA}	V
I_{I3}	Input current on nRE pin	0 V ≤ V_{IN} ≤ V_{CCA}	-10		10	μA
Common-mode transient immunity						
CMTI	Common-mode transient immunity	V_{CM} = 1200V See Figure 8-8 and 8-9	±150	±200		kV/us
Thermal Protection						
T_{SD}	Thermal shutdown threshold	Temperature rising		155		℃
T_{HYS}	Thermal shutdown hysteresis			10		℃

7.6 Switching Characteristics

7.6.1 Switching Characteristics—1Mbps

V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V, T_A = -40°C to 125°C, unless otherwise noted. All typical values are at 25°C and supply voltage of V_{CCA} = 5 V, V_{CCB} = 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
t_R, t_F	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 8-3		190	650	ns
t_{PHL}, t_{PLH}	Driver propagation delay time			175	400	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				20	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 8-4 and Figure 8-5			300	ns
t_{PZH}, t_{PZL}	Enable time				10	μs
Receiver						
t_R, t_F	Receiver output rise/fall time	C_L = 15 pF, see Figure 8-6		2.5		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			90	135	ns
$t_{SK(P)}$	Receiver output pulse skew,$\|t_{PHL} - t_{PLH}\|$				20	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	see Figure 8-7			100	ns
t_{PZL}, t_{PZH}	Receiver enable time				100	ns

7.6.2 Switching Characteristics—20Mbps

V_{CCA} = 3V to 5.5V, V_{CCB} = 3V to 5.5V, T_A = -40°C to 125°C, unless otherwise noted. All typical values are at 25°C and supply voltage of V_{CCA} = 5 V, V_{CCB} = 5 V.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver						
t_R, t_F	Driver differential output rise/fall time	R_L = 54 Ω, C_L = 50 pF, see Figure 8-3		6	20	ns
t_{PHL}, t_{PLH}	Driver propagation delay time			45	85	ns
$t_{SK(P)}$	Driver differential output pulse skew, $\|t_{PHL} - t_{PLH}\|$				15	ns
t_{PHZ}, t_{PLZ}	Disable time	See Figure 8-4 and Figure 8-5			260	ns
t_{PZH}, t_{PZL}	Enable time				10	μs
Receiver						
t_R, t_F	Receiver output rise/fall time	C_L = 15 pF, see Figure 8-6		2.5		ns
t_{PHL}, t_{PLH}	Receiver propagation delay time			60	90	ns
$t_{SK(P)}$	Receiver output pulse skew,$\|t_{PHL} - t_{PLH}\|$				15	ns
t_{PHZ}, t_{PLZ}	Receiver disable time	see Figure 8-7			100	ns
t_{PZL}, t_{PZH}	Receiver enable time				100	ns

8 Parameter Measurement Information

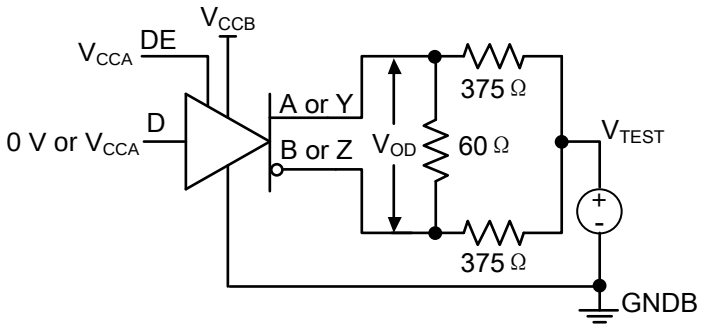


Figure 8-1. Measurement of Driver Differential Output Voltage With Common-Mode Load

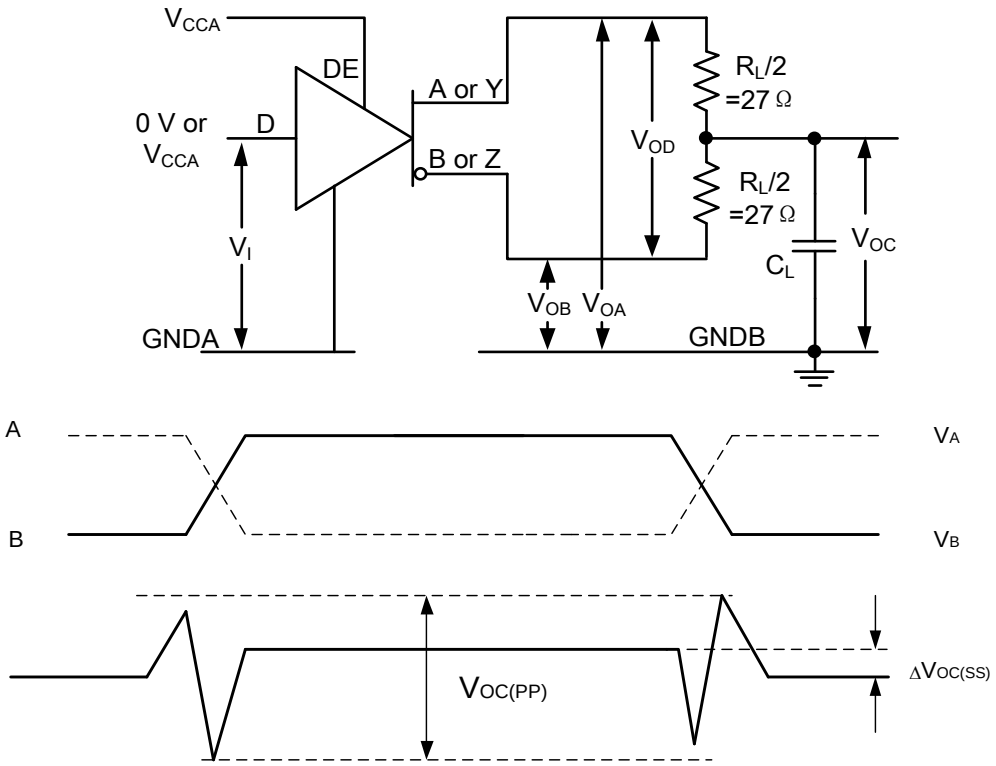


Figure 8-2. Measurement of Driver Differential and Common-Mode Output With RS-485 Load

8 Parameter Measurement Information (continued)

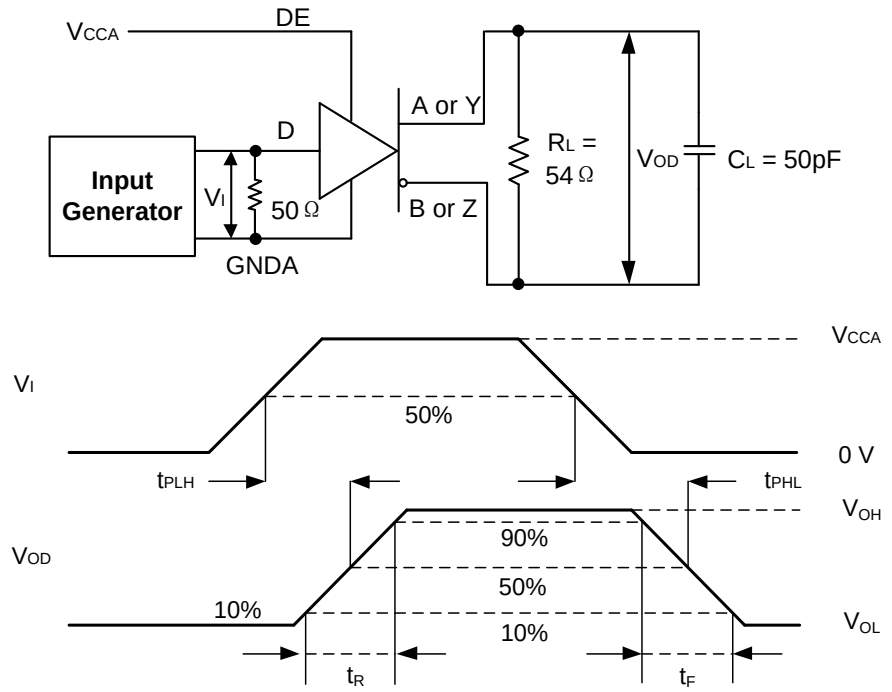


Figure 8-3. Measurement of Driver Differential Output Rise and Fall Times and Propagation Delays

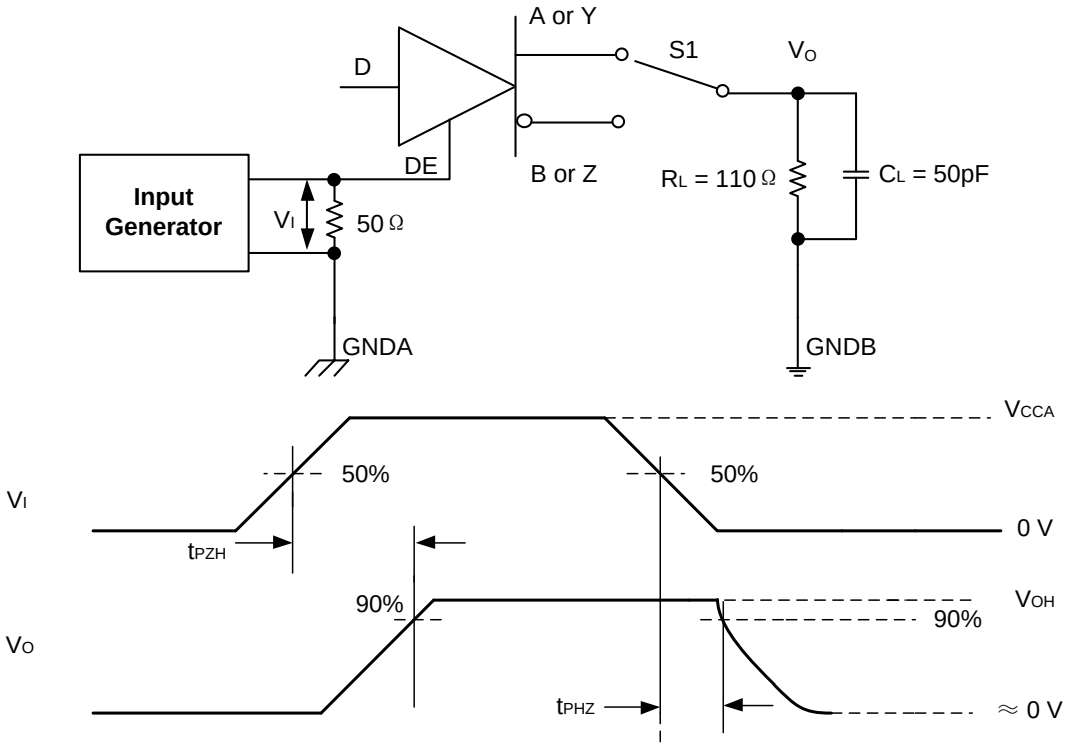


Figure 8-4. Driver Enable and Disable Times

8 Parameter Measurement Information (continued)

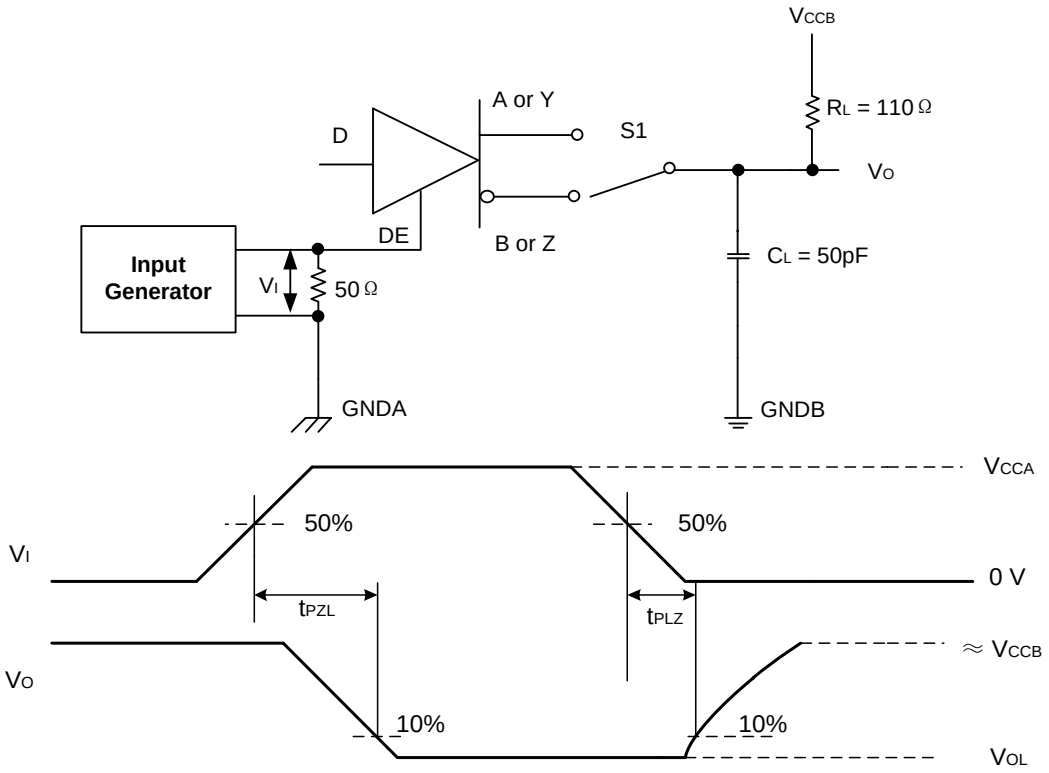


Figure 8-5. Driver Enable and Disable Times

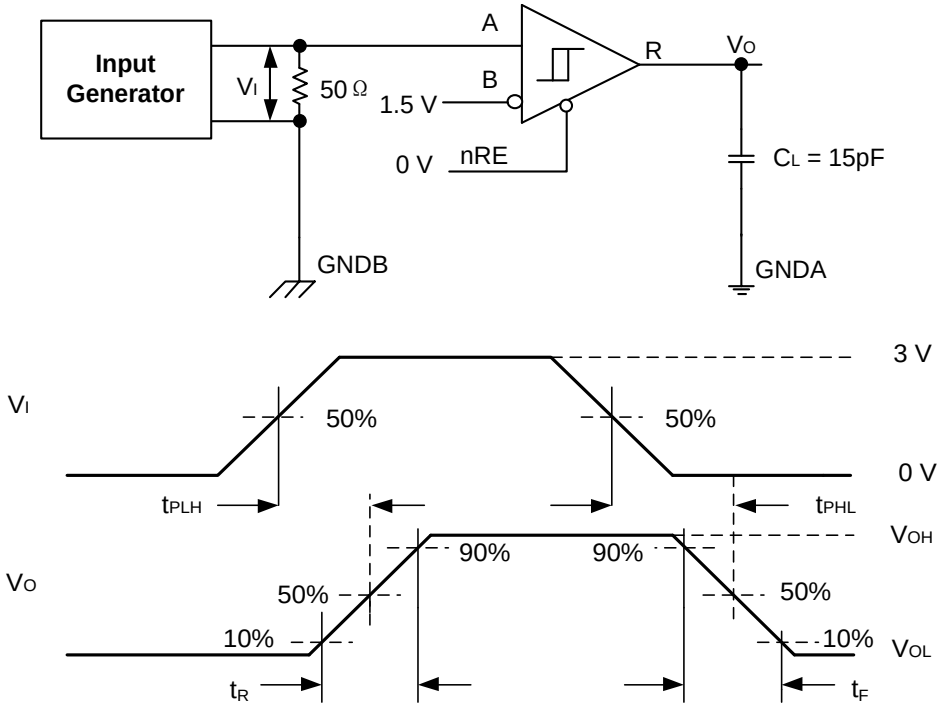


Figure 8-6. Measurement of Receiver Output Rise and Fall Times and Propagation Delays

8 Parameter Measurement Information (continued)

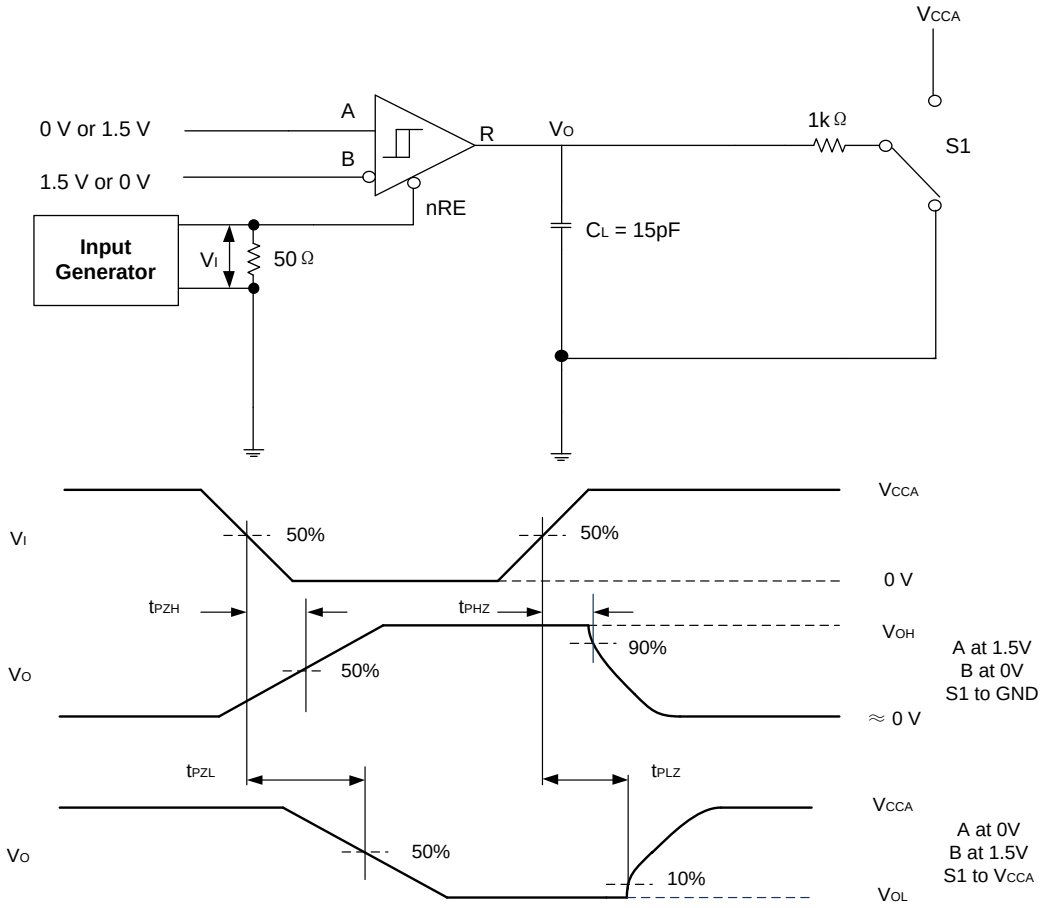


Figure 8-7. Receiver Enable and Disable Times

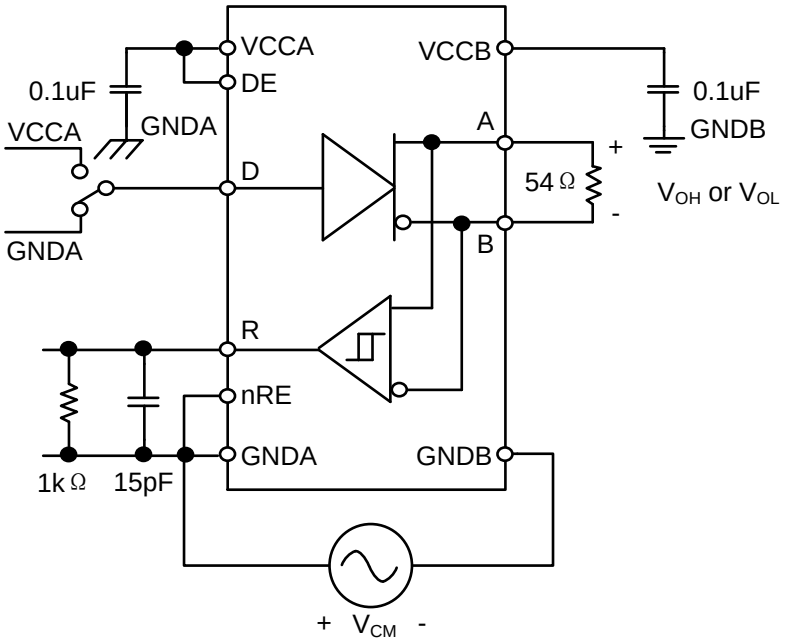


Figure 8-8. Half-Duplex Common-Mode Transient Immunity Test Circuit

8 Parameter Measurement Information (continued)

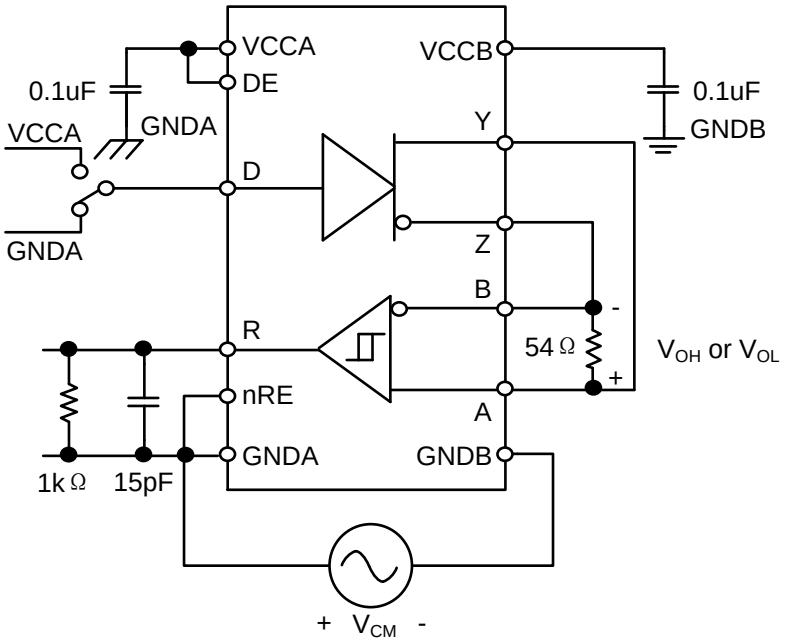


Figure 8-9. Full-Duplex Common-Mode Transient Immunity Test Circuit

9 Detailed Description

9.1 Overview

The UMISO3481, UMISO13082, UMISO3481F and UMISO13082F are isolated RS-485/RS-422 transceivers designed to operate in harsh industrial environments. The UMISO3481 and UMISO3481F support up to 1 Mbps. The UMISO13082 and UMISO13082F support up to 20 Mbps. The silicon-dioxide based capacitive isolation barrier supports an isolation withstand voltage of 5000V_{RMS} and an isolation working voltage of 1500 V_{PK}. Isolation breaks the ground loop between the communicating nodes and allows for data transfer in the presence of large ground potential differences. A minimum differential output voltage of 2.1 V is specified at a V_{CCB} voltage of 5V ±10% which meets the requirements for Profibus applications. The wide logic supply of the device (V_{CCA}) supports interfacing with 3.3-V, and 5-V control logic.

9.2 Functional Block Diagram

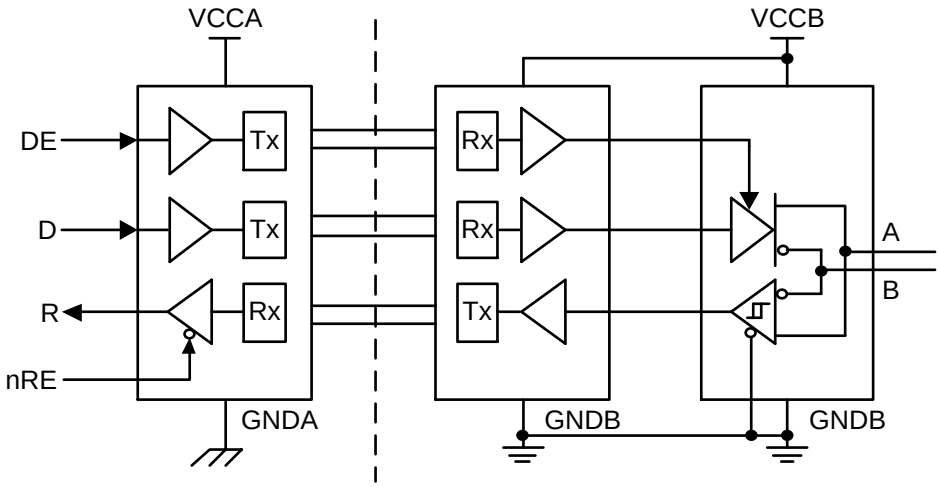


Figure 9-1. UMISO3481 and UMISO13082 Block Diagram

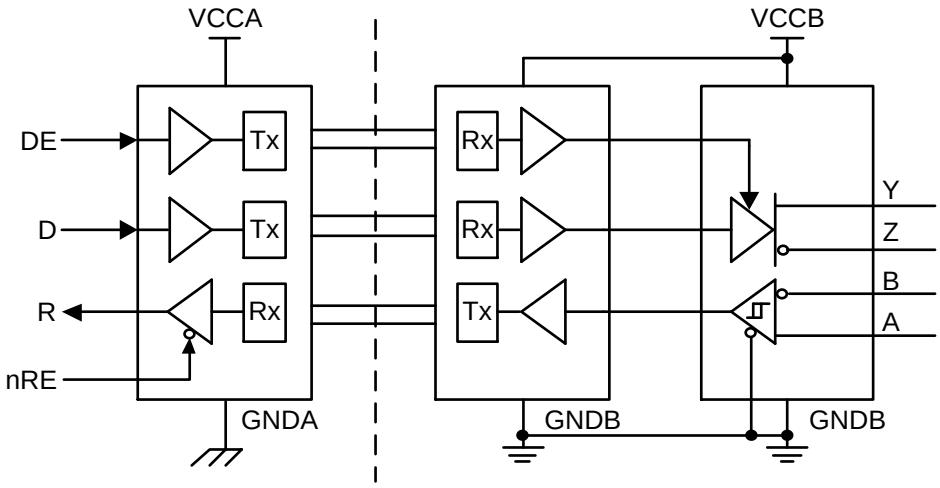


Figure 9-2. UMISO3481F and UMISO13082F Block Diagram

10 Feature Description

10.1 Thermal Shutdown

All devices have a thermal shutdown circuit to protect against damage when a fault condition occurs. A driver output short circuit or bus contention condition can cause the driver current to increase significantly which increases the power dissipation inside the device. An increase in the die temperature is monitored and the device is disabled when the die temperature becomes 155℃ (typical) which lets the device decrease the temperature. The device is enabled when the junction temperature becomes 145℃ (typical).

Bus short circuit for an extended duration and/or beyond voltage levels specified in recommended operating condition should be avoided. Repeated or prolonged exposure to bus shorts can result in high junction temperatures and affect device reliability.

10.2 Driver

The description that follows is specific to half-duplex device but the same logic applies to full-duplex device with the outputs being Y and Z.
When the driver enable pin, DE, is logic high, the differential outputs, A and B, follow the logic states at data input, D. A logic high at the DI input causes the A output to go high and the B output to go low. Therefore, the differential output voltage defined by Equation 1 is positive.

$$V_{OD} = V_A - V_B \quad (1)$$

A logic low at the D input causes the B output to go high and the A output to go low. Therefore, the differential output voltage defined by Equation 1 is negative. A logic low at the DE input causes both outputs to go to the high-impedance (Hi-Z) state. The logic state at the D pin is irrelevant when the DE input is logic low. The DE pin has an internal pulldown resistor to ground. The driver is disabled (bus outputs are in the Hi-Z) by default when the DE pin is left open. The D pin has an internal pull-up resistor. The A output goes high and the B output goes low when the D pin is left open while the driver enabled.

Table 10-1 shows the driver functional modes.

Table 10-1. Driver Function Table (Note 1, 2, 3)

VCCA	VCCB	D	DE	Outputs	
				Y, A	Z, B
PU	PU	H	H	H	L
		L	H	L	H
		X	L	Hi-Z	Hi-Z
		X	Open	Hi-Z	Hi-Z
		Open	X	H	L
PD	PU	X	X	Hi-Z	Hi-Z
X	PD	X	X	Hi-Z	Hi-Z

Note 1: PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state.
Note 2: A strongly driven input signal can weakly power the floating V_{CCA} through an internal protection diode and cause an undetermined
Note 3: The driver outputs are Y and Z for a full-duplex device. The driver outputs are A and B for a half-duplex device.

10.3 Receiver

The receiver is enabled when the receiver enable pin, nRE, is logic low. The receiver output, R, goes high when the differential input voltage defined by Equation 2 is greater than the positive input threshold, V_{TH+}.

$$V_{ID} = V_A - V_B \quad (2)$$

The receiver output, R, goes low when the differential input voltage defined by Equation 2 is less than the negative input threshold, V_{TH-}. If the V_{ID} voltage is between the V_{TH+} and V_{TH-} thresholds, the output is indeterminate. The receiver output is in the Hi-Z state and the magnitude and polarity of V_{ID} are irrelevant when the nRE pin is logic high or left open. The internal biasing of the receiver inputs causes the output to go to a failsafe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted to one another (short-circuit), or the bus is not actively driven (idle bus).

Table 10-2 shows the receiver functional modes

Table 10-2. Receiver Function Table (Note 1, 2)

V_{CCA}	V_{CCB}	Differential Input	nRE	R
PU	PU	$V_{TH+} \leq V_A - V_B$	L	H
		$V_{TH-} < V_A - V_B < V_{TH+}$	L	Indeterminate
		$V_A - V_B \leq V_{TH-}$	L	L
		X	H	Hi-Z
		X	Open	Hi-Z
		Open, Short, Idle	L	H
PD	PU	X	X	Hi-Z
PU	PD	X	L	H

Note 1: PU = Powered Up; PD = Powered Down; H = High Level; L = Low level; X = Irrelevant, Hi-Z = High impedance state.
Note 2: A strongly driven input signal can weakly power the floating V_{CCA} through an internal protection diode and cause an undetermined output.

10.4 Receiver Fail-Safe Operation

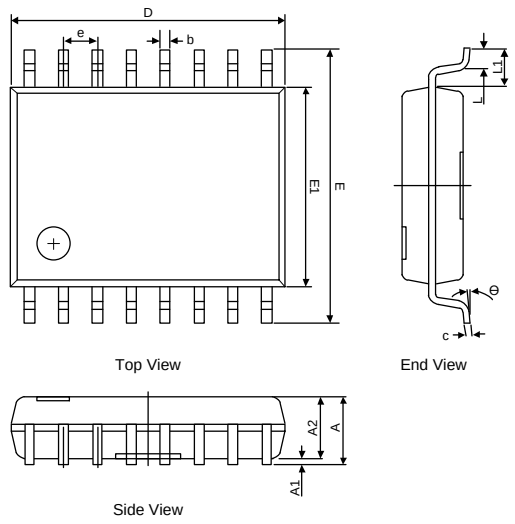
The receivers are fail-safe to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

11 Package Information

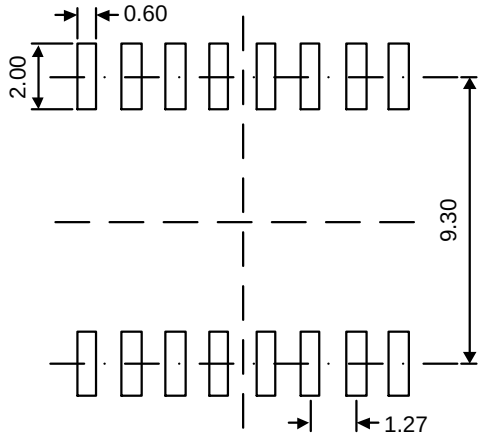
WSOP16

Outline Drawing



DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	2.65	-	-	0.104
A1	0.10	-	0.30	0.004	-	0.012
A2	2.25	-	2.35	0.089	-	0.093
b	0.35	-	0.43	0.014	-	0.017
c	0.24	-	0.29	0.009	-	0.011
D	10.2	10.3	10.4	0.402	0.406	0.409
E	10.1	10.3	10.5	0.398	0.406	0.413
E1	7.4	7.5	7.6	0.291	0.295	0.299
e	1.27BSC			0.050 BSC		
L	0.55	-	0.85	0.022	-	0.033
L1	1.40REF			0.060REF		
θ	0 °	-	8 °	0 °	-	8 °

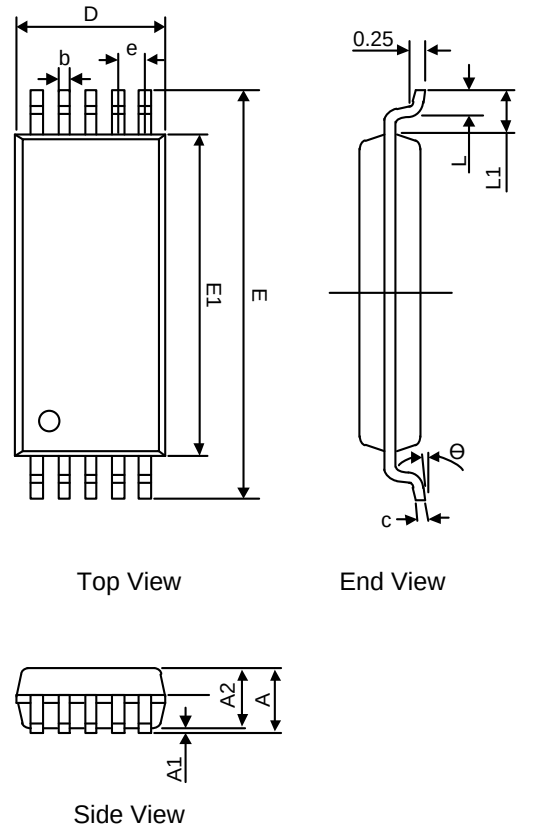
Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

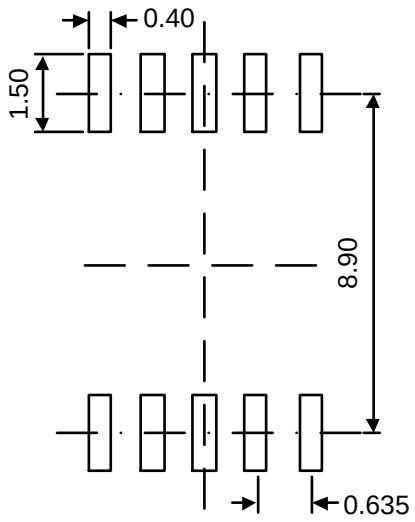
WSSOP10

Outline Drawing



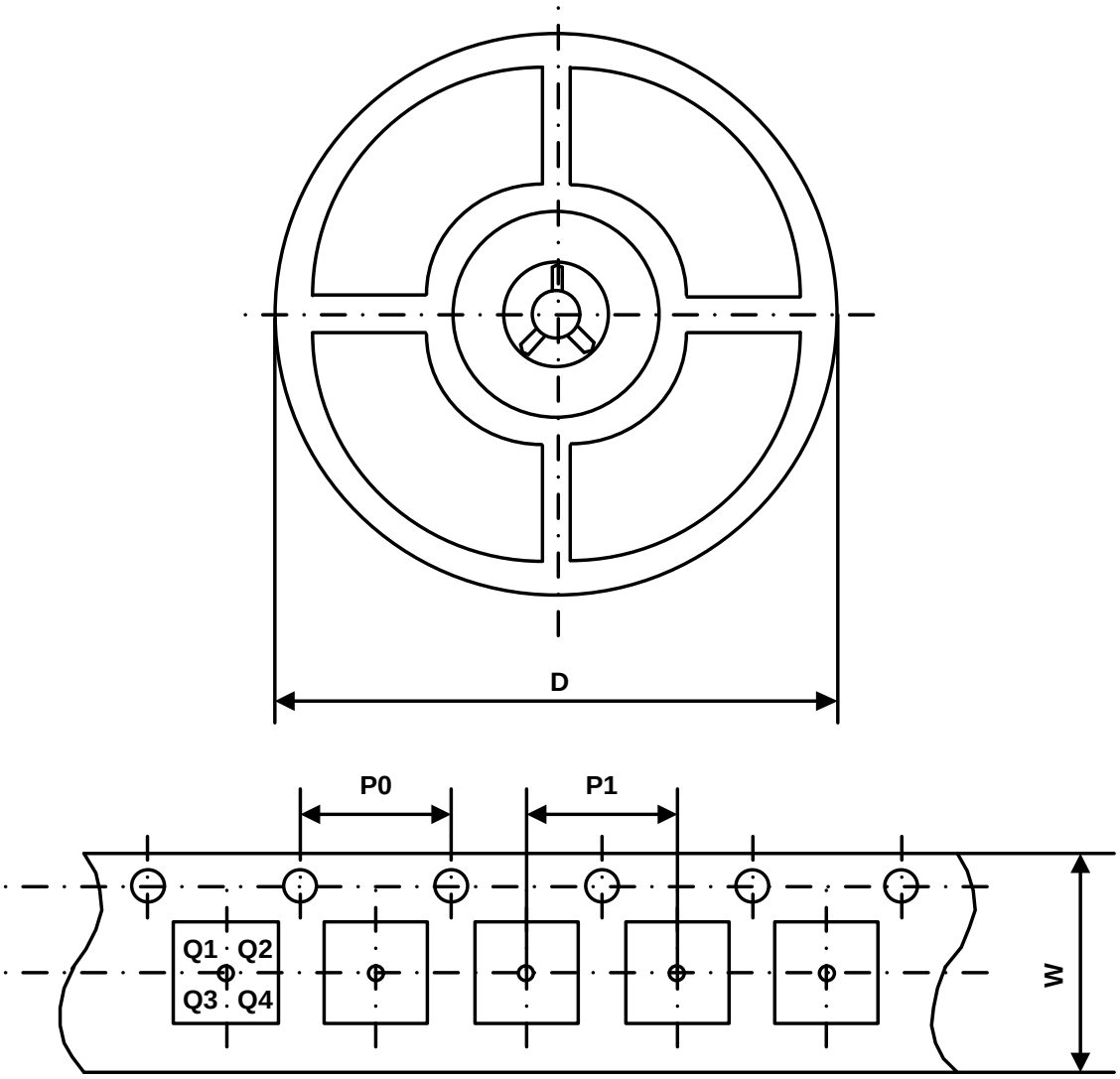
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.65	-	-	0.066
A1	0.05	-	0.20	0.002	-	0.008
A2	1.35	1.40	1.45	0.054	0.056	0.058
b	0.23	-	0.31	0.009	-	0.013
c	0.20	-	0.24	0.008	-	0.009
D	3.40	3.50	3.60	0.136	0.140	0.144
E	9.30	9.50	9.70	0.372	0.380	0.388
E1	7.40	7.50	7.60	0.296	0.300	0.304
e	0.635BSC			0.0254BSC		
L	0.45	-	0.75	0.018	-	0.030
L1	1.00REF			0.040REF		
θ	0°	-	7°	0°	-	7°

Land Pattern



NOTES:
1. Unit: mm;
2. General tolerance ±0.05mm unless otherwise specified;
3. The layout is just for reference.

12 Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UMISO3481WAB	WSSOP10	16 mm	4 mm	8 mm	330 mm	Q2
UMISO3481WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO13082WAB	WSSOP10	16 mm	4 mm	8 mm	330 mm	Q2
UMISO13082WSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO3481FWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1
UMISO13082FWSG	WSOP16	16 mm	4 mm	12 mm	330 mm	Q1

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