

Quad Channel Low Capacitance ESD Protection Array

UM5404EEDF DFN6 1.6×1.6

General Description

UM5404EEDF is surge rated diode arrays designed to protect high speed data interfaces. This series has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage caused by ESD (electrostatic discharge), electrical fast transients (EFT) and lighting.

The unique design incorporates surge rated, low capacitance steering diodes and a TVS diode in a single package. During transient conditions, the steering diodes direct the transient to either the positive side of the power supply line or to ground. The internal TVS diode prevents over-voltage on the power line, protecting any downstream components.

UM5404EEDF has a low typical capacitance of 1pF and operates with virtually no insertion loss to 2GHz. This makes the device ideal for protection of high-speed data line such as USB2.0, Firewire, DVI and gigabit Ethernet interface.

The low capacitance array configuration allows the user to protect four high-speed data or transmission lines. The low inductance construction minimizes voltage overshoot during high current surges. This device is optimized for ESD protection of portable electronics. They may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

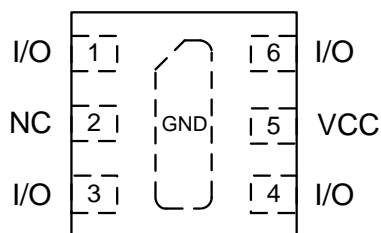
Applications

- USB 2.0
- USB OTG
- 10/100/1000Mbit Ethernet
- Monitors and Flat Panel Displays
- Digital Visual Interface (DVI)
- High-Definition Multimedia Interface (HDMI)
- SIM Ports
- IEEE 1394 Firewire Ports

Features

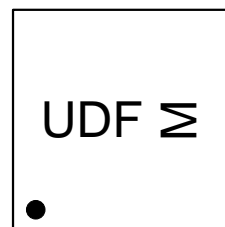
- Transient Protection for High-Speed Data Lines to
IEC 61000-4-2 (ESD) $\pm 20\text{kV}$ (Air), $\pm 12\text{kV}$ (Contact)
- IEC 61000-4-4 (EFT) 40A (5/50ns)
- IEC 61000-4-5 (Lighting) 10A (8/20 μs)
- Array of Surge Rated Diodes with Internal TVS Diode
- Protects up to Four I/O Lines & Power Line
- Low Capacitance ($<1\text{pF}$) for High-Speed Interfaces, No Insertion Loss to 2.0GHz
- Low Leakage Current and Clamping Voltage
- Low Operating Voltage: 5.0V

Pin Configurations



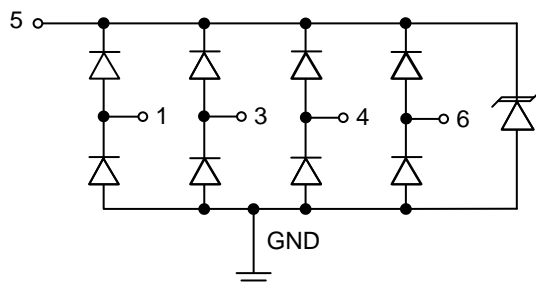
(Top View)

Top View



M: Month Code
UM5404EEDF
DFN6 1.6×1.6

Circuit Diagram



Pin Configurations

Pin Number	Symbol	Function
1, 3, 4, 6	I/O	Input/Output Lines
2	NC	Not Connected
5	VCC	Supply Voltage
Center Tab	GND	Ground

Ordering Information

Part Number	Working Voltage	Packaging Type	Channel	Marking Code	Shipping Qty
UM5404EEDF	5.0V	DFN6 1.6×1.6	4	UDF	3000pcs/7 Inch Tape & Reel

Absolute Maximum Ratings

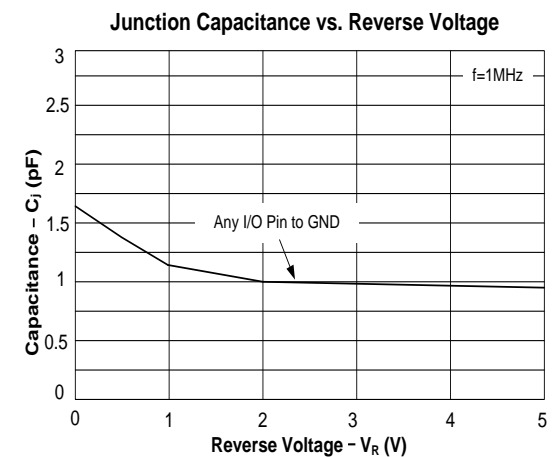
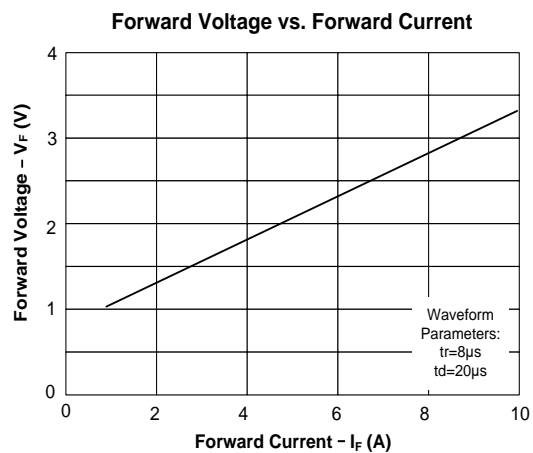
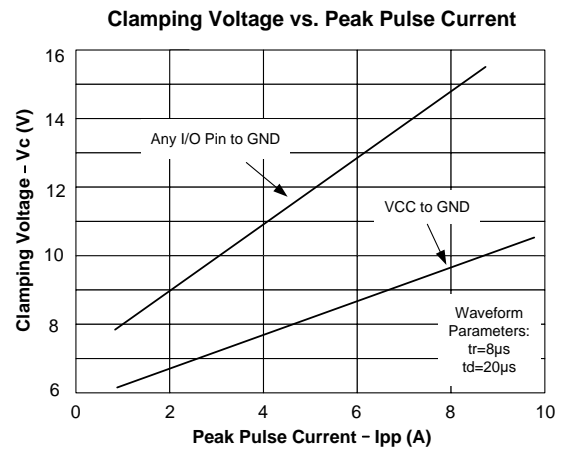
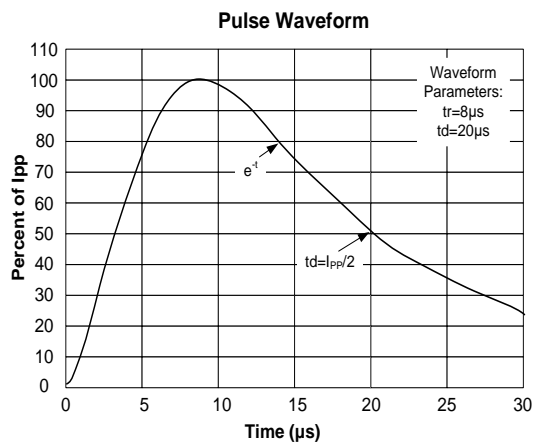
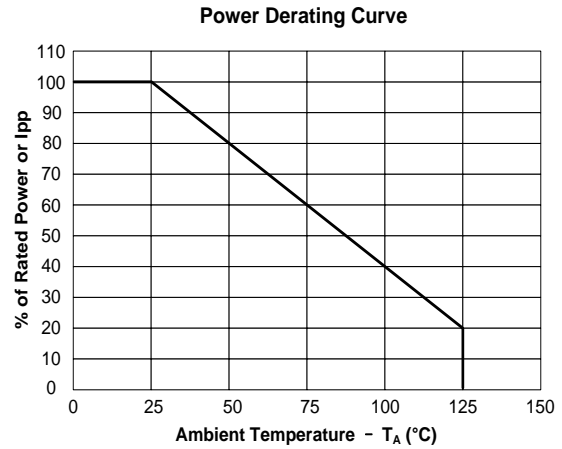
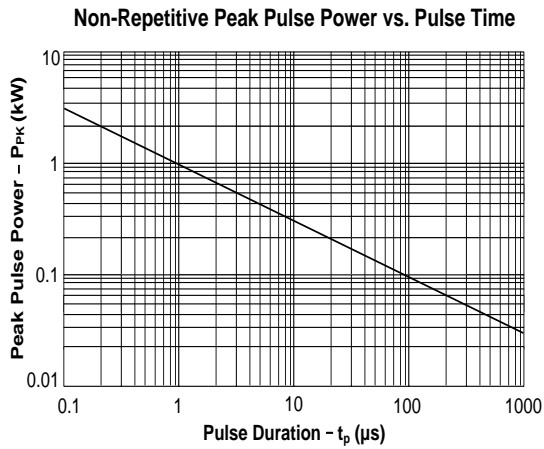
Rating	Symbol	Value	Unit
Peak Pulse Power ($t_p=8/20\mu s$)	P_{pk}	200	Watts
Peak Pulse Current ($t_p=8/20\mu s$)	I_{pp}	10	A
Peak Pulse Current ($t_p=5/50ns$)	I_{pp}	40	A
ESD per IEC 61000-4-2 (Air) ESD per IEC 61000-4-2 (Contact)	V_{ESD}	± 20 ± 12	kV
Operating Temperature	T_J	-55 to +125	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical Characteristics (Note 1)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Reverse Stand-Off Voltage	V_{RWM}	VCC to GND			5.0	V
Reverse Breakdown Voltage	V_{BR}	$I_T=1mA$, VCC to GND	6.0			V
Reverse Leakage Current	I_R	$V_{RWM}=5V$, VCC to GND			2	μA
Clamping Voltage	V_C	$I_{PP}=1A$, 8/20 μs Any I/O Pin to GND		8	10	V
Clamping Voltage	V_C	$I_{PP}=5A$, 8/20 μs Any I/O Pin to GND		12	15	V
Junction Capacitance	C_j	$V_R=0V$, $f=1MHz$ Any I/O Pin to GND			2	pF
		$V_R=0V$, $f=1MHz$, Between I/O Pins			1	pF
		$V_R=0V$, $f=1MHz$ VCC to GND		60		pF
		$V_R=2.5V$, $f=1MHz$ VCC to GND		40		pF
Reverse Recovery Time	T_{rr}	Any I/O Pin to VCC		130		ns
		GND to VCC		300		ns
		GND to any I/O Pin		400		ns

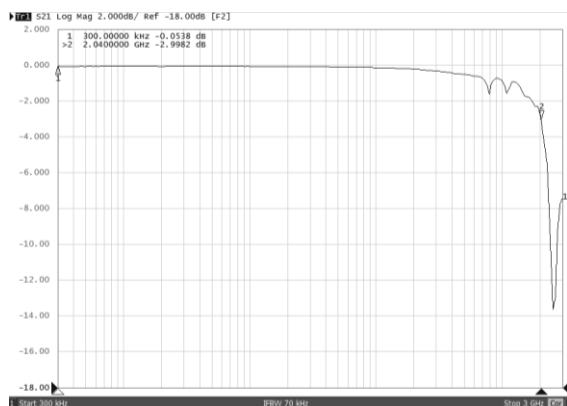
Note 1: I/O pins are pin 1, 3, 4, and 6.

Typical Operating Characteristics

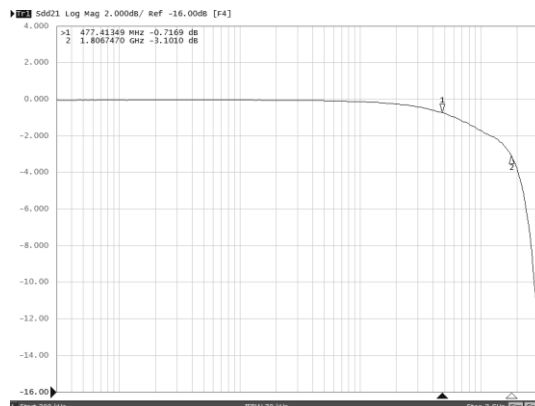


Typical Operating Characteristics (Continued)

Single End Bandwidth



Differential Bandwidth



Crosstalk

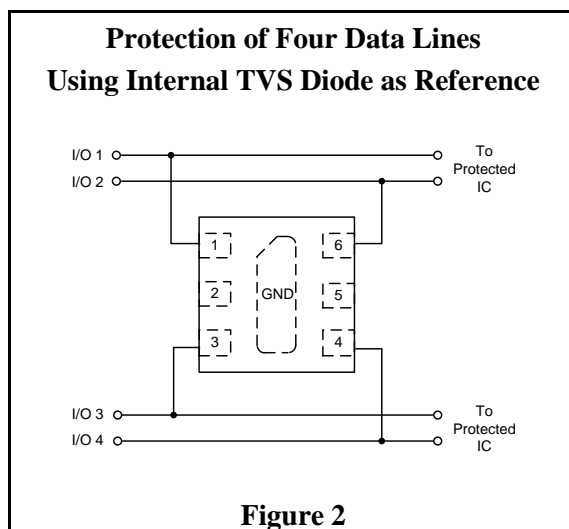
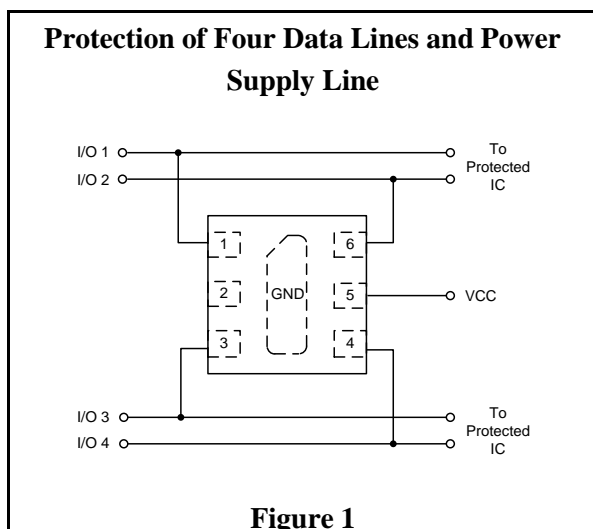


Applications Information

Device Connection Options for Protection of Four High-Speed Data Lines

This device is designed to protect four data lines by clamping them to a fixed reference. When the voltage on the protected line exceeds the reference voltage the steering diodes are forward biased, conducting the transient current away from the sensitive circuitry. Data lines are connected at I/O pins. The center GND pin should be connected directly to a ground plane. The path length is kept as short as possible to minimize parasitic inductance. NC pin is not connected. The positive reference is connected at VCC pin. The options for connecting the positive reference are as follows:

1. To protect data lines and the power line, connect VCC pin directly to the positive supply rail (VCC). In this configuration the data lines are referenced to the supply voltage. The internal TVS diode prevents over-voltage on the supply rail. See Figure 1.
2. In applications where the supply rail does not exit the system, the internal TVS may be used as the reference. In this case, VCC pin is not connected. The steering diodes will begin to conduct when the voltage on the protected line exceeds the working voltage of the TVS (plus one diode drop).
3. In applications where complete supply isolation is desired, the internal TVS is again used as the reference and VCC is connected to one of the I/O inputs. An example of this configuration is the protection of a SIM port. The Clock, Reset, I/O, and VCC lines are connected at I/O pins. GND pin is connected to ground, NC and VCC pins are not connected. See Figure 2.



Universal Serial Bus ESD Protection

The UM5404EEDF may also be used to protect the USB ports on monitors, computers, peripherals or portable systems. Each device will protect up to two USB ports (Figure 3). When the voltage on the data lines exceed the bus voltage (plus one diode drop), the internal rectifiers are forward biased conducting the transient current away from the protected controller chip. The TVS diode directs the surge to ground. The TVS diode also acts to suppress ESD strikes directly on the voltage bus. Thus, both power and data pins are protected with a single device.

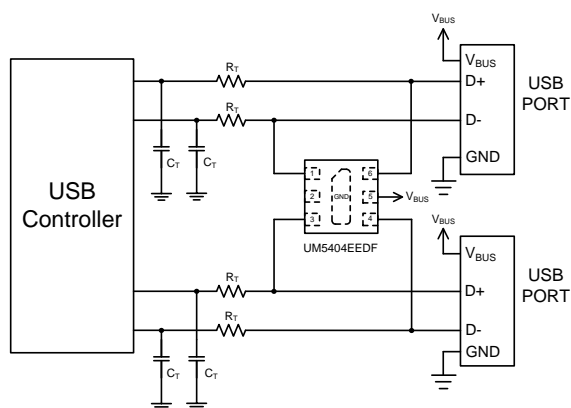


Figure 3 Dual USB Port Protection

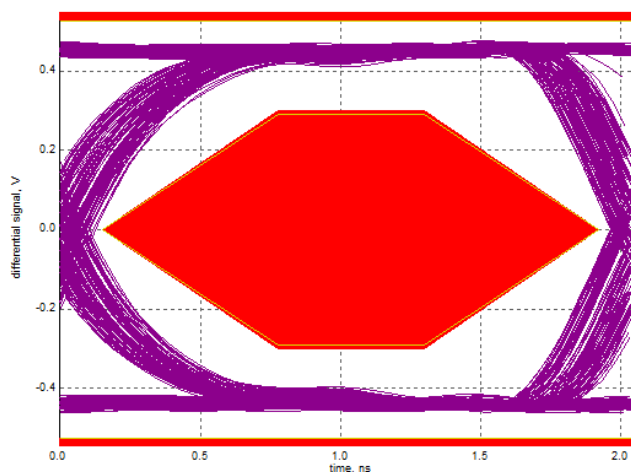


Figure 4 USB Eye Diagram

Note: Figure 4 is tested by the MSO9254A oscilloscope of Agilent including E2678 probe, 1169 differential probe and E2645B-66401 fixture, when the chip is linked into the data line.

10/100 Ethernet Protection

Ethernet ICs are vulnerable to damage from electrostatic discharge (ESD). The internal protection in the PHY chip, if any, often is not enough due to the high energy of the discharges specified by IEC61000-4-2. If the discharge is catastrophic, it will destroy the protected IC. If it is less severe, it will cause latent failures that are very difficult to find.

10/100 Ethernet operates at 125MHz clock over a twisted pair interface. In a typical system, the twisted pair interface for each port consists of two differential signal pairs: one for the transmitter and one for the receiver, with the transmitter input being the most sensitive to damage. The fatal discharge occurs differentially across the transmitter or receiver line pair and is capacitively coupled through the transformer to the Ethernet chip. Figure 5 shows how to design the UM5404EEDF on the line side of a 10/100 ethernet port to provide differential mode protection. The common mode isolation of the transformer will provide common mode protection to the rating of the transformer isolation which is usually >1.5kV. If more common mode protection is needed, figure 6 shows how to design the UM5404EEDF on the IC side of the 10/100 Ethernet circuit to provide differential and common mode protection. The UM5404EEDF can not be grounded on the line side because the hi-pot test requires the line side not to be grounded.

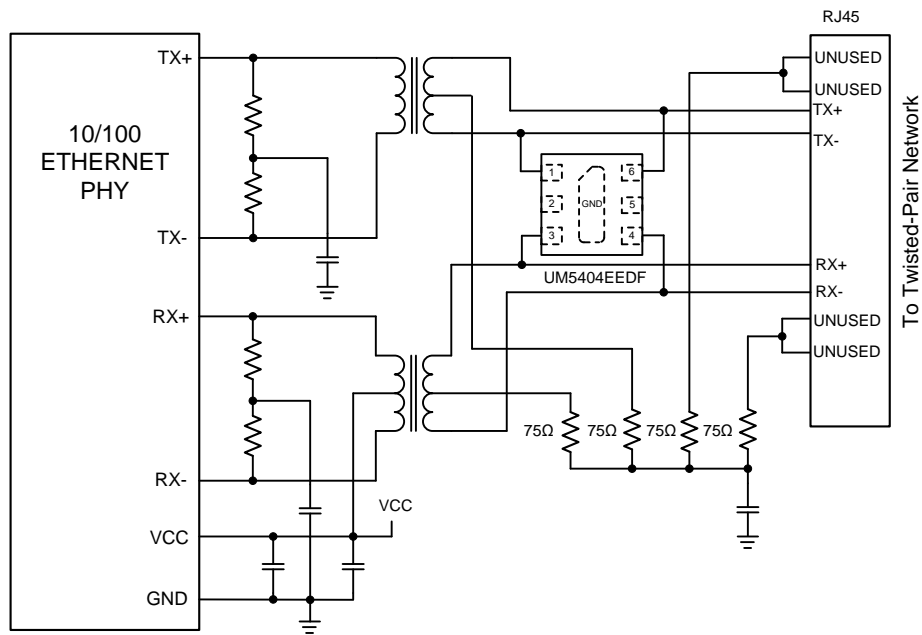


Figure 5 10/100 Ethernet Differential Protection

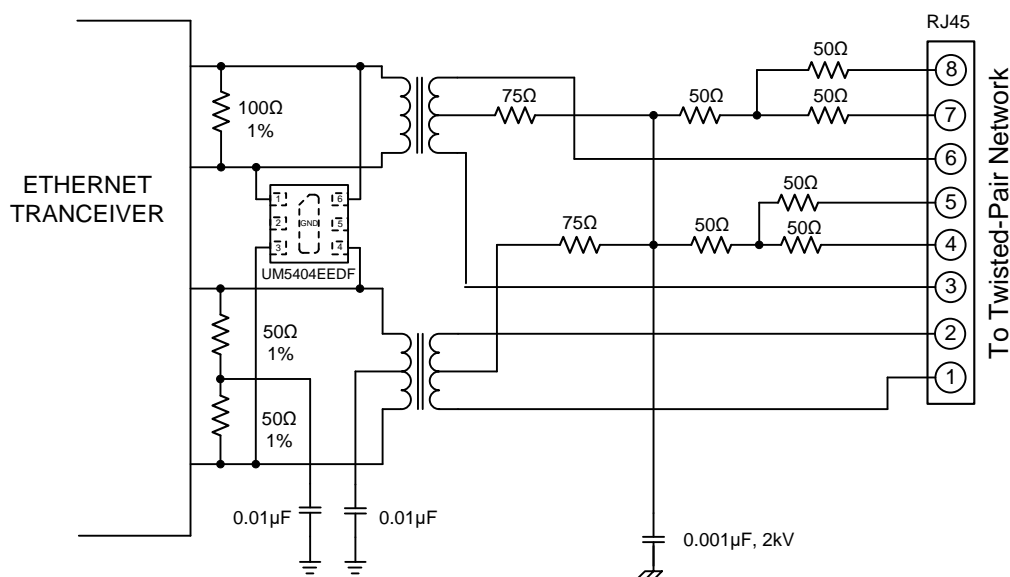


Figure 6 10/100 Ethernet Differential and Common Mode Protection

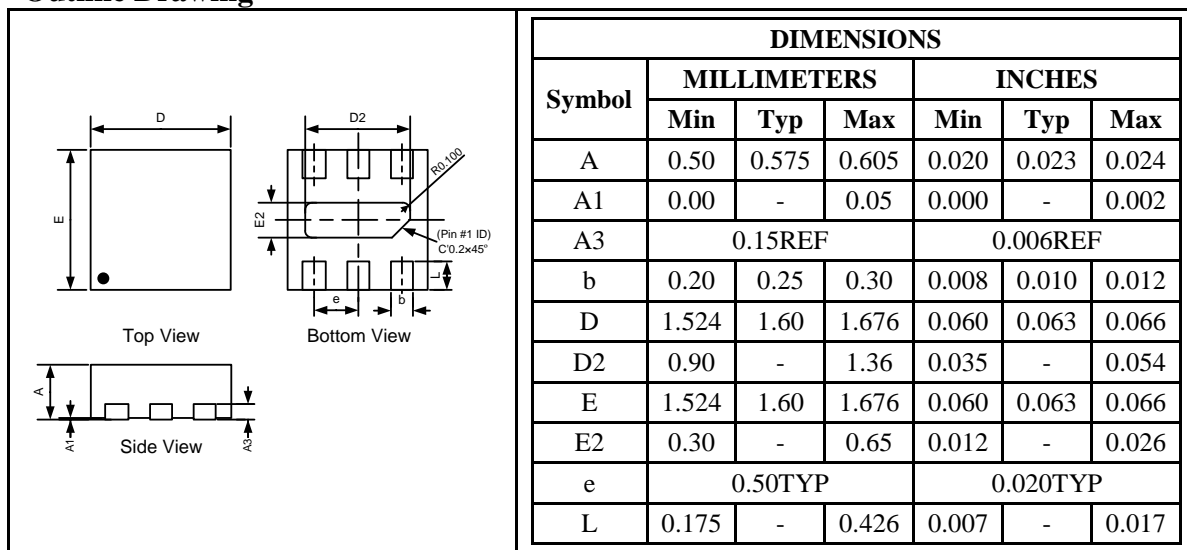
Matte Tin Lead Finish

Matte tin has become the industry standard lead-free replacement for SnPb lead finishes. A matte tin finish is composed of 100% tin solder with large grains. Since the solder volume on the leads is small compared to the solder paste volume that is placed on the land pattern of the PCB, the reflow profile will be determined by the requirements of the solder paste. Therefore, these devices are compatible with both lead-free and SnPb assembly techniques. In addition, unlike other lead-free compositions, matte tin does not have any added alloys that can cause degradation of the solder joint.

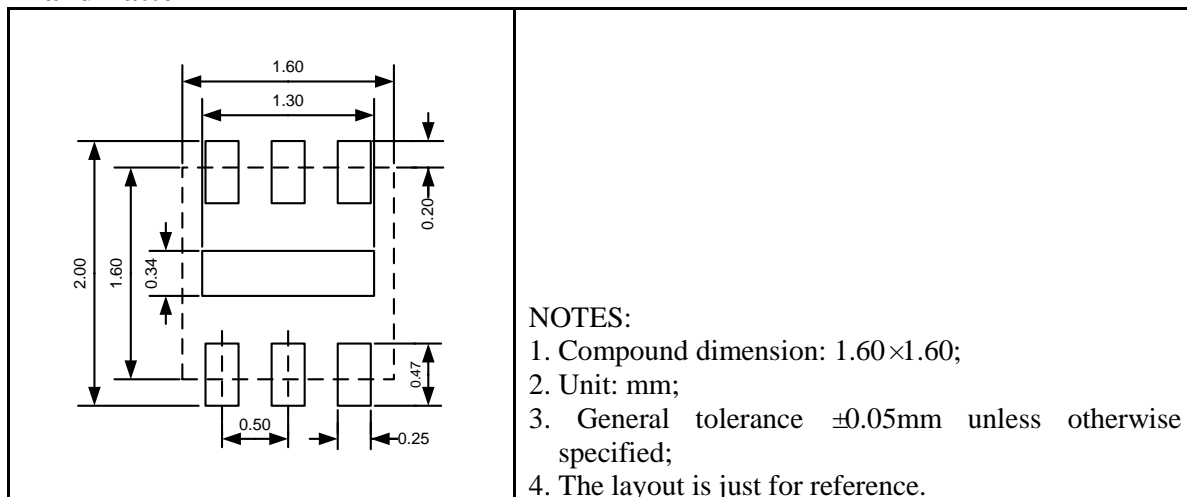
Package Information

UM5404EEDF DFN6 1.6×1.6

Outline Drawing



Land Pattern



Tape and Reel Orientation



GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.

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