

2-Bit Dual-Supply Bidirectional I²C/I²C Bus and SPI Voltage Translator

UM3A9606 DFN8 1.4×1.0

1 Description

The UM3A9606 is a 2-bit, dual-supply bidirectional I²C, I²C, SMBus and SPI voltage-level translator with auto direction sensing. The device features one output enable input (OE) and 0.72V to 1.98V power supply on both A-side and B-side which makes it suitable for low voltage nodes (0.8V, 1.2V, 1.8V). In addition, $V_{CCA} \leq V_{CCB}$ for proper operation.

The UM3A9606 can be used for both open-drain and push-pull application which is compatible with I²C, 12.5 MHz I²C-Bus applications and higher speed SPI applications.

Pins An are referenced to V_{CCA} and Pins Bn are referenced to V_{CCB} . The OE pin is referenced to V_{CCA} and set to low to place An and Bn pins in high-impedence state. The device also supports partial power-down applications using I_{OFF}. The I_{OFF} circuit disables the outputs to prevent the backflow current through the device.

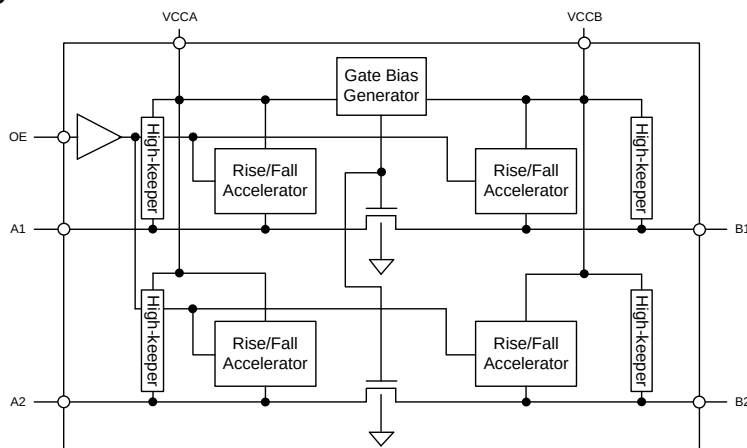
2 Applications

- Servers
- Wearables
- Personal electronics

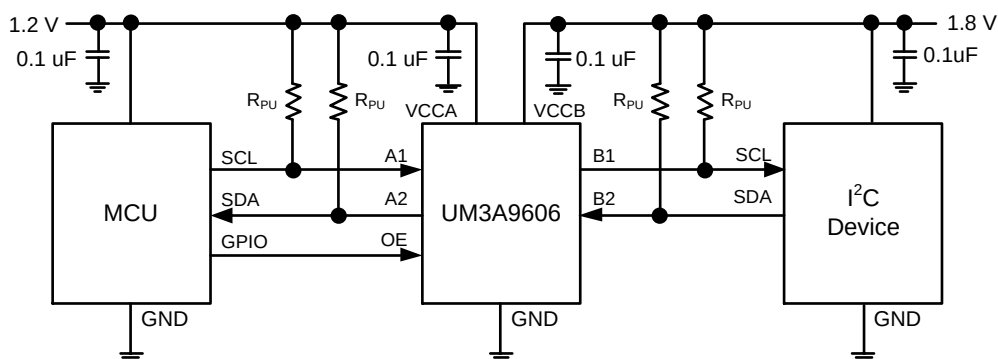
3 Features

- 2-bit, dual-supply bidirectional translator for I²C, I²C, SMBus and SPI applications
- Wide supply voltage:
 - V_{CCA} : 0.72 V to 1.98V
 - V_{CCB} : 0.72 V to 1.98V, $V_{CCA} \leq V_{CCB}$
- Compatible with MIPI I²C supporting speeds up to 12.5MHz
- I_{OFF} supports partial power-down mode operation
- V_{CC} isolation feature – if either V_{CC} input is at GND, all are in the high-impedance state
- Latch-up performance exceeds 200 mA per JESD 78, Class II
- ESD protection
 - ±8kV Human body model (HBM)
 - ±2kV Charged-device model (CDM)

4 Block Diagram



5 Typical Application Schematic



6 Ordering Information

Part Number	Mark Code	Package Type	Shipping Qty
UM3A9606DA8	PJ	DFN8 1.4×1.0	3000pcs/7Inch Tape & Reel

7 Pin Configuration and Function

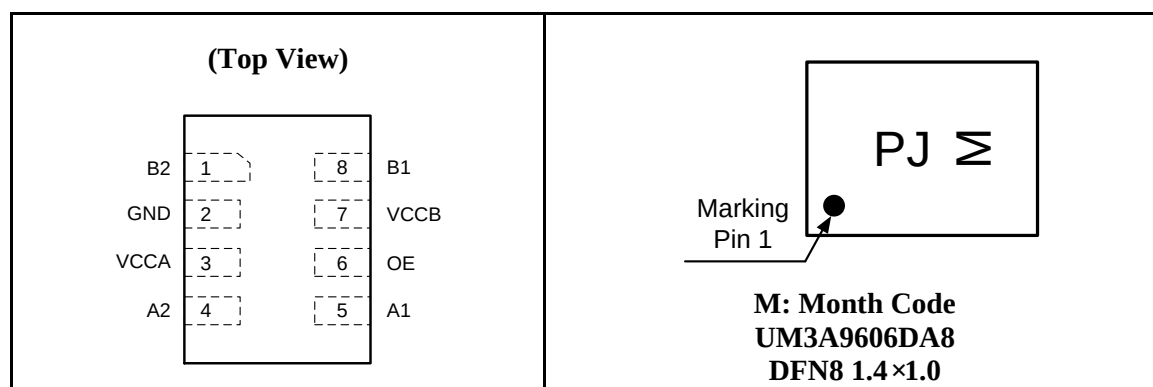


Table 7-1. Pin Functions

Pin No.	Pin Name	Function
1	B2	Input/output B2. Referenced to V_{CCB} .
2	GND	Ground.
3	VCCA	A-port supply voltage. $0.72V \leq V_{CCA} \leq 1.98 V$.
4	A2	Input/output A2. Referenced to V_{CCA} .
5	A1	Input/output A1. Referenced to V_{CCA} .
6	OE	Output enable input (active high, referenced to V_{CCA}); signal can be from V_{CCA} or V_{CCB} domain.
7	VCCB	B-port supply voltage. $0.72V \leq V_{CCB} \leq 1.98 V$, $V_{CCA} \leq V_{CCB}$.
8	B1	Input/output B1. Referenced to V_{CCB} .

8 Specifications

8.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCA}	Supply voltage	V _{CCA} ≤ V _{CCB}	-0.5	2.5	V
V _{CCB}	Supply voltage	V _{CCA} ≤ V _{CCB}	-0.5	2.5	V
V _I	Input voltage (Note 2)	A port, B port, and OE	-0.5	2.5	V
V _O	Output voltage (Note 2, 3, 4)	Active mode	-0.5	V _{CCO}	V
		Power-down or 3-state mode	-0.5	2.5	V
I _{IK}	Input clamp current	V _I < 0 V	-50		mA
I _{OK}	Output clamp current	V _O < 0 V	-50		mA
I _O	Output current (Note 3)	V _O = 0 V to V _{CCO}		±50	mA
I _{CC}	Supply current	I _{CCA} or I _{CCB}		100	mA
I _{GND}	Ground current		-100		mA
T _{STG}	Storage temperature		-65	+150	°C
P _{TOT}	Total power dissipation	T _A = -40 °C to +125 °C		125	mW

Note 1: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: The minimum input and minimum output voltage ratings can be exceeded if the input and output current ratings are observed.

Note 3: V_{CCO} is the supply voltage associated with the output.

Note 4: V_{CCO} + 0.25 V should not exceed 2.5 V.

8.2 Recommended operating conditions (Note 1)

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CCA}	Supply voltage	V _{CCA} ≤ V _{CCB}	0.72	1.98	V
V _{CCB}	Supply voltage	V _{CCA} ≤ V _{CCB}	0.72	1.98	V
V _I	Input voltage	A port, B port, and OE	0	1.98	V
V _O	Output voltage (Note 2, 3, 4)	Power-down or 3-state mode; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V	0	1.98	V
		A port or B port	0	1.98	V
Δt/ΔV	Input transition rise and fall rate	V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		5.3	ns/V
T _A	Ambient temperature		-40	125	°C

Note 1: The A and B sides of an unused I/O pair must be held in the same state, both at V_{CCI} or both at GND.

8.3 Thermal Information

Symbol	Parameter		Value	Unit
$R_{\theta JA}$	Junction to ambient thermal resistance	DFN8 1.4×1.0	114.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	DFN8 1.4×1.0	1.6	°C/W

8.4 Typical Electrical Characteristics (Static)

Over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and voltages are referenced to GND.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	A port; $V_{CCA} = 1.2\text{ V}$; $I_O = -15\text{ }\mu\text{A}$		1.05		V
V_{OL}	Low-level output voltage (Note 1)	A port; $V_{CCA} = 1.2\text{ V}$; $I_O = 20\text{ }\mu\text{A}$		0.09		V
I_I	Input leakage current	OE input; $V_I = 0\text{ V}$ or 1.98 V ; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 0.72\text{ V}$ to 1.98 V	-1		1	μA
I_{OZ}	OFF-state output current (Note 2)	A or B port ; $V_O = 0\text{ V}$ to V_{CCO} ; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 0.72\text{ V}$ to 1.98 V	-1		1	μA
I_{OFF}	Power off leakage current	A port; V_I or $V_O = 0\text{ V}$ to 1.98 V ; $V_{CCA} = 0\text{ V}$; $V_{CCB} = 0\text{ V}$ to 1.98 V	-1		1	μA
		B port; V_I or $V_O = 0\text{ V}$ to 1.98 V ; $V_{CCB} = 0\text{ V}$; $V_{CCA} = 0\text{ V}$ to 1.98 V	-1		1	μA
I_{CC}	Supply current	$V_I = 0\text{ V}$ or V_{CCI} ; $I_O = 0\text{ A}$ (Note 3)				
		I_{CCA} ; $V_{CCA} = 0.72\text{ V}$; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		0.05		μA
		I_{CCB} ; $V_{CCA} = 0.72\text{ V}$; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		0.5		μA
		$I_{CCA} + I_{CCB}$; $V_{CCA} = 0.72\text{ V}$; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		0.6		μA
C_I	Input capacitance	OE input; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		1.0		pF
$C_{I/O}$	Input/output capacitance	A port; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		4.0		pF
		B port; $V_{CCA} = 0.72\text{ V}$ to 1.98 V ; $V_{CCB} = 0.72\text{ V}$ to 1.98 V		4.0		pF

Note 1: When $V_I = 0.05\text{ V}$, $I_O = 15\text{ }\mu\text{A}$, $R_{ON(MAX)} = 250\text{ }\Omega$ ($V_{CCA} > 0.9\text{ V}$), $R_{ON(MAX)} = 370\text{ }\Omega$ ($V_{CCA} < 0.9\text{ V}$), the low output voltage can be calculated as $V_{OL} = V_I + I_O \times R_{ON(MAX)}$.

Note 2: V_{CCO} is the supply voltage associated with the output.

Note 3: V_{CCI} is the supply voltage associated with the input.

8.5 Electrical Characteristics (Static)

Over operating free-air temperature range (unless otherwise noted). Voltages are referenced to GND.

Symbol	Parameter	Conditions	-40°C to +85°C		-40°C to +125°C		Unit
			Min	Max	Min	Max	
V_{IH}	High-level input voltage (Note 1)	A or B port					
		$V_{CCA} = 0.72\text{ V to }1.32\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.32\text{ V}$	$V_{CCI}-0.15$		$V_{CCI}-0.15$		V
		$V_{CCA} = 1.32\text{ V to }1.98\text{ V};$ $V_{CCB} = 1.32\text{ V to }1.98\text{ V}$	$V_{CCI}-0.2$		$V_{CCI}-0.2$		V
		OE input					
		$V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.98\text{ V}$	$0.65 \times V_{CCA}$		$0.65 \times V_{CCA}$		V
V_{IL}	Low-level input voltage	A or B port					
		$V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.98\text{ V}$		$0.2 \times V_{CCI}$		$0.2 \times V_{CCI}$	V
		OE input					
		$V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.98\text{ V}$		$0.3 \times V_{CCA}$		$0.3 \times V_{CCA}$	V
V_{OH}	High-level output voltage (Note 2, 3)	A port; $V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $I_O = -15\text{ }\mu\text{A}$	$V_{CCO}-0.195$		$V_{CCO}-0.195$		V
		B port; $V_{CCB} = 0.72\text{ V to }1.98\text{ V};$ $I_O = -15\text{ }\mu\text{A}$	$V_{CCO}-0.195$		$V_{CCO}-0.195$		V
V_{OL}	Low-level output voltage (Note 2, 4)	A port; $V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_I = 0.05\text{ V}, I_O = 15\text{ }\mu\text{A}$		0.3		0.3	V
		B port; $V_{CCB} = 0.72\text{ V to }1.98\text{ V};$ $V_I = 0.05\text{ V}, I_O = 15\text{ }\mu\text{A}$		0.3		0.3	V
I_I	Input leakage current	OE input; $V_I = 0\text{ V to }1.98\text{ V};$ $V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.98\text{ V}$	-2	+2	-5	+5	μA
I_{OZ}	OFF-state output current (Note 2)	A or B port; $V_O = 0\text{ V or }V_{CCO};$ $V_{CCA} = 0.72\text{ V to }1.98\text{ V};$ $V_{CCB} = 0.72\text{ V to }1.98\text{ V}$	-2	+2	-10	+10	μA
I_{OFF}	Power off leakage current	A port; $V_I \text{ or } V_O = 0\text{ V to }1.98\text{ V};$ $V_{CCA} = 0\text{ V};$ $V_{CCB} = 0\text{ V to }1.98\text{ V}$	-2	+2	-10	+10	μA
		B port; $V_I \text{ or } V_O = 0\text{ V to }1.98\text{ V};$ $V_{CCB} = 0\text{ V};$ $V_{CCA} = 0\text{ V to }1.98\text{ V}$	-2	+2	-10	+10	μA

8.5 Electrical Characteristics (Static) (continued)

Over operating free-air temperature range (unless otherwise noted). All typical values are at 25°C and voltages are referenced to GND.

Symbol	Parameter	Conditions	-40°C to +85°C		-40°C to +125°C		Unit
			Min	Max	Min	Max	
I _{CC}	Supply current	I _{CCA} ; V _I = 0 V or V _{CCI} ; I _O = 0 A (Note 1)					
		OE = Low; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		5		15	μA
		OE = High; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		6		20	μA
		V _{CCA} = 1.98 V; V _{CCB} = 0 V		3.5		15	μA
		V _{CCA} = 0 V; V _{CCB} = 1.98 V		-2		-15	μA
		I _{CCB} ; V _I = 0 V or V _{CCI} ; I _O = 0 A (Note 1)					
		OE = Low; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		8		29	μA
		OE = High; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		11		36	μA
		V _{CCA} = 1.98 V; V _{CCB} = 0 V		-2		-15	μA
		V _{CCA} = 0 V; V _{CCB} = 1.98 V		6		20	μA
		I _{CCA} + I _{CCB} ; V _I = 0 V or V _{CCI} ; I _O = 0 A (Note 1)					
		OE = Low; V _{CCA} = 0.72 V to 1.98 V; V _{CCB} = 0.72 V to 1.98 V		16		56	μA

Note 1: V_{CCI} is the supply voltage associated with the input.

Note 2: V_{CCO} is the supply voltage associated with the output.

Note 3: The V_{OH(MIN)} can be calculated by V_{CCO} - I_O × 10 kΩ × 1.3. The 1.3 factor is for the design margin. In this case, I_O = 15 μA and R_{PU} = 10 kΩ then V_{OH(MIN)} = V_{CCO} - 0.195 V.

Note 4: When V_I = 0.05 V, I_O = 15 μA, R_{ON(MAX)} = 250 Ω (V_{CCA} > 0.9 V), R_{ON(MAX)} = 370 Ω (V_{CCA} < 0.9 V), the low output voltage can be calculated as V_{OL} = V_I + I_O × R_{ON(MAX)}.

8.6 Dynamic Characteristics for temperature range -40 °C to +125 °C

Voltages are referenced to GND ; see Figure 9-1 for test circuit; see Figure 9-2 and Figure 9-3 for waveforms.

Symbol	Parameter	Conditions	V _{CCB} = 1.2 V ±10%			V _{CCB} = 1.8 V ±10%			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CCA} = 0.8 V ±10%									
t _{PD}	Propagation delay (Note 1)	A to B; C _L = 15 pF	2.1	5.6	10.5	1.7	3.9	15	ns
		B to A; C _L = 15 pF	1.2	10.6	19.9	0.5	9.6	17.2	ns
t _{EN}	Enable time	OE to A, B; C _L = 15 pF	16	125	210	16	120	240	ns
t _{DIS}	Disable time (Note 2)	OE to A; C _L = 15 pF			600			600	ns
		OE to B; C _L = 15 pF			600			600	ns
t _T	Transition time	A port; C _L = 15 pF	2.1	8.5	17.5	1.5	9	15.4	ns
		B port; C _L = 15 pF	1.1	4	18	0.7	1.5	18	ns
t _{SK(O)}	Output skew time (Note 3)	Delta between channels	0.0	0.2	0.4	0.0	0.2	0.4	ns
t _W	Pulse width	Data inputs	37			37			ns
f _{DATA}	Data rate		0.064		24	0.064		18	Mbit/s
V _{CCA} = 1.2 V ±10%									
t _{PD}	Propagation delay (Note 1)	A to B; C _L = 15 pF	1.5	4.5	6.2	1.0	2.5	4.8	ns
		B to A; C _L = 15 pF	1.1	3.9	5.4	0.6	2.8	4.8	ns
t _{EN}	Enable time	OE to A, B; C _L = 15 pF	3	50	135	3	50	135	ns
t _{DIS}	Disable time (Note 2)	OE to A; C _L = 15 pF			600			600	ns
		OE to B; C _L = 15 pF			600			600	ns
t _T	Transition time	A port; C _L = 15 pF	0.8	2.6	4.9	0.6	1.5	4	ns
		B port; C _L = 15 pF	1.1	3.6	5.1	0.6	1.3	4.5	ns
t _{SK(O)}	Output skew time (Note 3)	Delta between channels	0.0	0.1	0.3	0.0	0.1	0.3	ns
t _W	Pulse width	Data inputs	15			13.5			ns
f _{DATA}	Data rate		0.064		52	0.064		52	Mbit/s

Note 1: t_{PD} is the same as t_{PLH} and t_{PHL}; t_{EN} is the same as t_{PZL} and t_{PZH}; t_{DIS} is the same as t_{PLZ} and t_{PHZ}; t_T is the same as t_{THL} and t_{TLH}.

Note 2: Guaranteed by design.

Note 3: Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

8.6 Dynamic Characteristics for temperature range -40 °C to +125 °C (continued)

Voltages are referenced to GND ; see Figure 9-1 for test circuit; see Figure 9-2 and Figure 9-3 for waveforms.

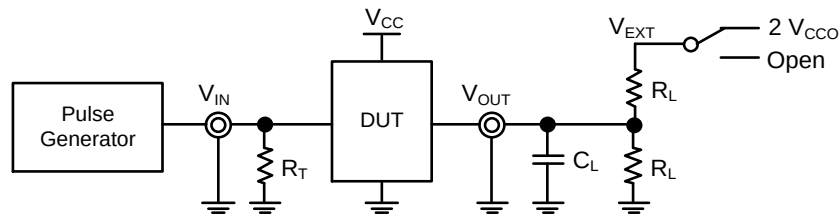
Symbol	Parameter	Conditions	V _{CCB} = 1.8 V ± 10%			Unit
			Min	Typ	Max	
V _{CCA} = 1.8 V ± 10%						
t _{PD}	Propagation delay (Note 1)	A to B; C _L = 15 pF	1.0	2.5	3.6	ns
		B to A; C _L = 15 pF	0.7	2.3	3.6	ns
t _{EN}	Enable time	OE to A, B; C _L = 15 pF	2	25	50	ns
t _{DIS}	Disable time (Note 2)	OE to A; C _L = 15 pF			600	ns
		OE to B; C _L = 15 pF			600	ns
t _T	Transition time	A port; C _L = 15 pF	0.5	1.2	3.2	ns
		B port; C _L = 15 pF	0.7	1.7	3.2	ns
t _{SK(O)}	Output skew time (Note 3)	Delta between channels	0.0	0.1	0.2	ns
t _W	Pulse width	Data inputs	13.5			ns
f _{DATA}	Data rate		0.064		52	Mbit/s

Note 1: t_{PD} is the same as t_{PLH} and t_{PHL} ; t_{EN} is the same as t_{PZL} and t_{PZH} ; t_{DIS} is the same as t_{PLZ} and t_{PHZ} ; t_T is the same as t_{THL} and t_{TLH} .

Note 2: Guaranteed by design.

Note 3: Skew between any two outputs of the same package switching in the same direction. One channel is not always faster than the other.

9 Parameter Measurement Information



Note 1: Load resistance $R_L = 1 \text{ M}\Omega$ for measuring data rate, pulse width, propagation delay and output rise and fall measurements. $R_L = 50 \text{ k}\Omega$ for measuring enable and disable times.

Note 2: R_T termination resistance should be equal to Z_{OUT} of pulse generators.

Note 3: C_L Load capacitance includes probe and jig capacitance. $C_L = 15 \text{ pF}$ when on the B-side.

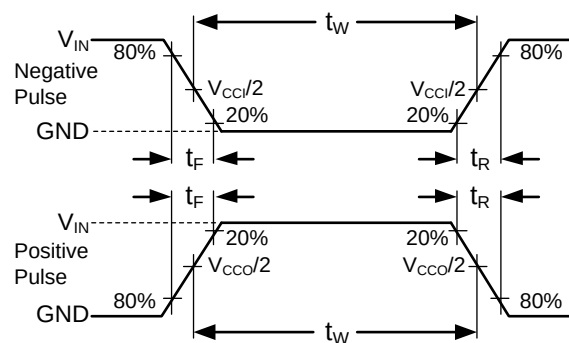
Note 4: V_{EXT} External voltage for measuring switching times.

Note 5: All input pulses are supplied by generators having the following characteristics: $PRR \leq 26 \text{ MHz}$, $Z_O = 50 \text{ }\Omega$, slew rate $\geq 1 \text{ V/ns}$.

Note 6: V_{CCI} is the V_{CC} associated with the input port.

Note 7: V_{CCO} is the V_{CC} associated with the output port.

Figure 9-1. Load Circuit



Note 1: All input pulses are supplied by generators having the following characteristics: $PRR \leq 26 \text{ MHz}$, $Z_O = 50 \text{ }\Omega$, slew rate $\geq 1 \text{ V/ns}$.

Note 2: $R_L = \text{Load resistance}$.

Note 3: C_L Load capacitance includes probe and jig capacitance.

Note 4: V_{EXT} External voltage for measuring switching times.

Figure 9-2. Test Circuit for Measuring Switching Times

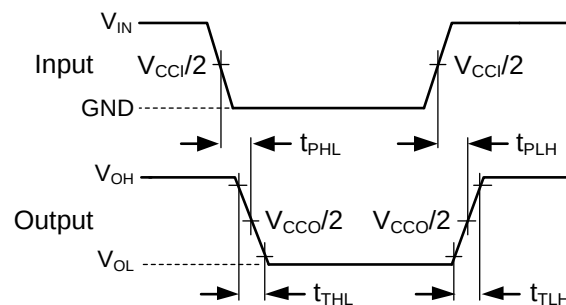
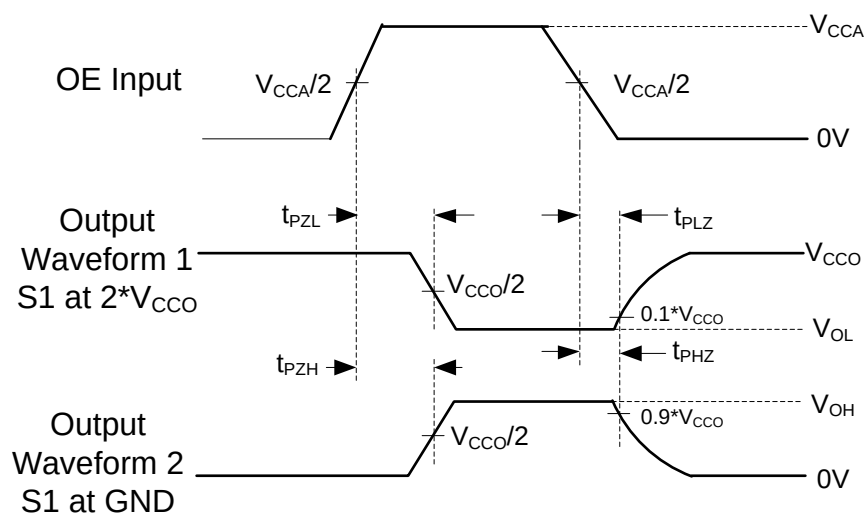


Figure 9-3. Propagation Delay Times

9 Parameter Measurement Information (continued)



Note 1: C_L includes probe and jig capacitance.

Note 2: Waveform 1 in Figure 9-4 is for an output with internal such that the output is high, except when OE is high.

Note 3: Waveform 2 in Figure 9-4 is for an output with conditions such that the output is low, except when OE is high.

Note 4: All input pulses are supplied by generators having the following characteristics: $PRR \leq 26$ MHz, $Z_O = 50 \Omega$, slew rate ≥ 1 V/ns.

Note 5: The outputs are measured one at a time, with one transition per measurement.

Note 6: t_{PLZ} and t_{PHZ} are the same as t_{DIS} .

Note 7: t_{PZL} and t_{PZH} are the same as t_{EN} .

Note 8: t_{PLH} and t_{PHL} are the same as t_{PD} .

Note 9: V_{CCI} is the V_{CC} associated with the input port.

Note 10: V_{CCO} is the V_{CC} associated with the output port.

Figure 9-4. Enable and Disable Times

10 Application and Implementation

10.1 Application Information

The UM3A9606 can be used to interface between devices or systems operating at different supply voltages. See Figure 10-1, Figure 10-2, and Figure 10-3 for a typical operating circuit using the UM3A9606.

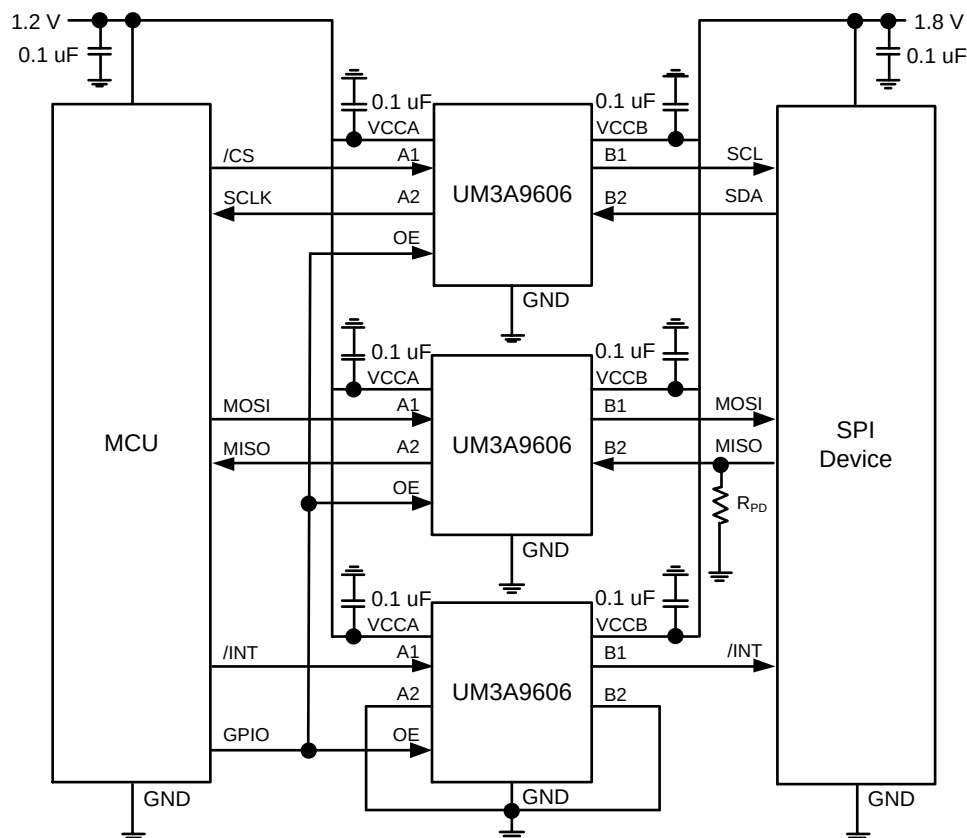


Figure 10-1. SPI application block diagram

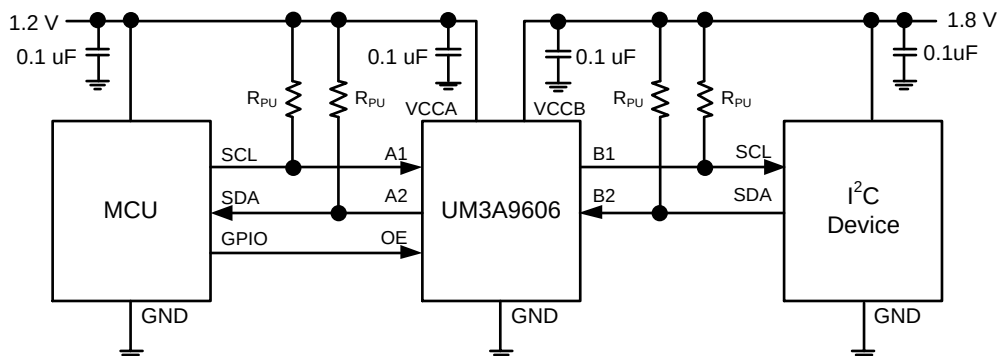


Figure 10-2. I²C application block diagram

10.1 Application Information (continued)

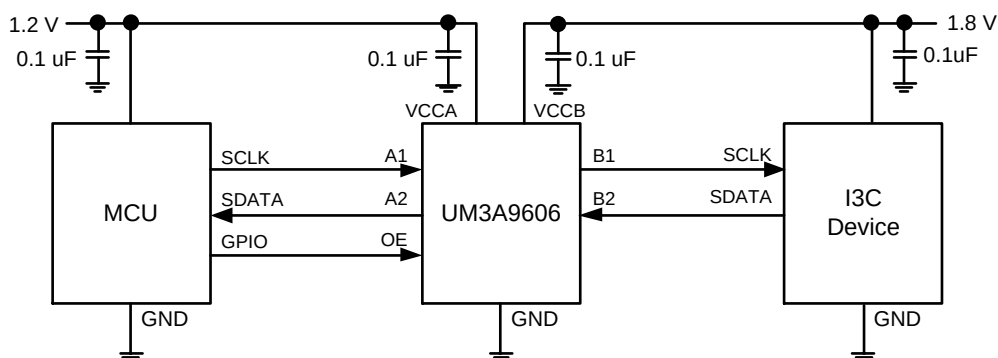


Figure 10-3. I3C application block diagram

10.2 Architecture

The architecture uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high), N-channel pass gate transistor and a pull-up resistor (to provide DC-bias and drive capabilities) to meet these requirements. The design is directionless and does not need a direction control signal. The implementation supports both low speed open-drain operation as well as high-speed push-pull operation. The N-channel pass gate transistor is on only during the low input cycle and is off during the high input cycle.

10.3 Input driver requirements

The continuous DC-current sinking or sourcing capability is determined by the external system-level; open-drain or push-pull drivers that are interfaced to the UM3A9606 I/O pins. The high bandwidth of these I/O circuits used to facilitate this fast change from an input to an output and an output to an input, they have a modest sourcing capability of hundreds of micro-amperes, as determined by the pull-up resistor. The fall time of a signal depends on the edge-rate and output impedance of the external driving the UM3A9606 data IOs, and the capacitive loading at the data lines.

10.4 Power-up and Power-down

This section outlines the power up and power-down sequence of the UM3A9606.

10.4.1 Power-up sequence

Turn on V_{CCB} first to the recommended operating voltage range, then turn on V_{CCA} .

10.4.2 Power-down sequence

Turn off V_{CCB} first, and after it is completely off, then turn off V_{CCA} . The different sequencing of each power supply does not damage the device during the power up operation. The UM3A9606 includes circuitry that disables all output ports and puts the device into a power-down mode when either V_{CCA} or V_{CCB} is switched off.

10.5 Enable and disable

An output enable input (OE) is used to enable/disable the device when both V_{CCA} and V_{CCB} are in recommended operating conditions. Setting OE = Low causes all I/Os to assume the high-impedance OFF state. The disable time (t_{DIS} with no external load) indicates the delay between when OE goes Low and when outputs actually become disabled. The enable time (t_{EN}) indicates the amount of time the user must allow for the one-shot circuitry to become operational after OE is taken High. To ensure the high-impedance OFF state during power up or power down, pin OE should be tied to GND; OE pin should not be left floating in any condition.

V_{IL} and V_{IH} of OE pin are referenced to V_{CCA} . The OE can be controlled by an external device that is powered by either V_{CCA} or V_{CCB} . As V_{CCB} is required to be greater than V_{CCA} , the OE pin has been designed to withstand a voltage equal to V_{CCB} (up to 1.98 V per recommended functional voltage range).

10.6 Layout guidelines

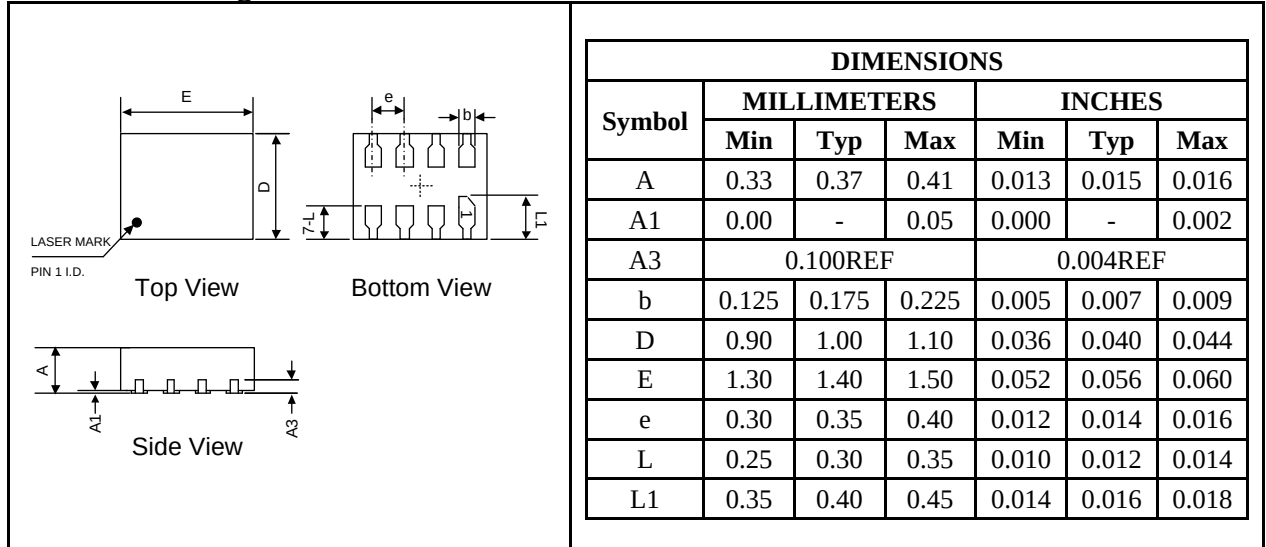
To ensure reliability of the device, the following common printed-circuit board (PCB) layout guidelines are recommended:

- Bypass capacitors must be used on power supplies and must be placed as close as possible to V_{CCA} , V_{CCB} and GND pins.
- Short trace lengths should be used to avoid excessive loading.
- PCB signal trace-lengths must be kept short enough so that the round-trip delay of any reflection is less than the one-shot duration, approximately 8 ns, ensuring that any reflection encounters low impedance at the source driver.

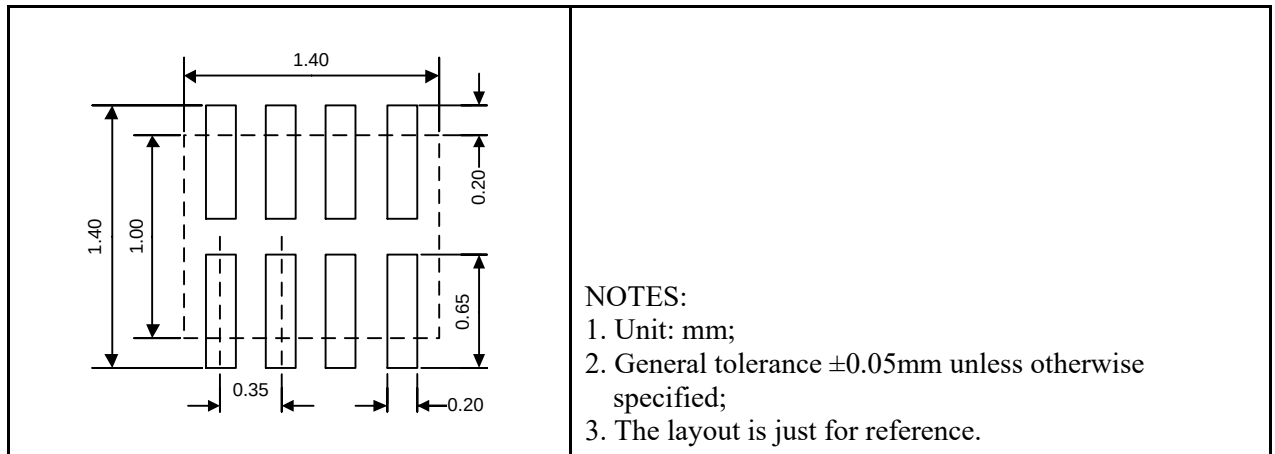
11 Package Information

DFN8 1.4×1.0

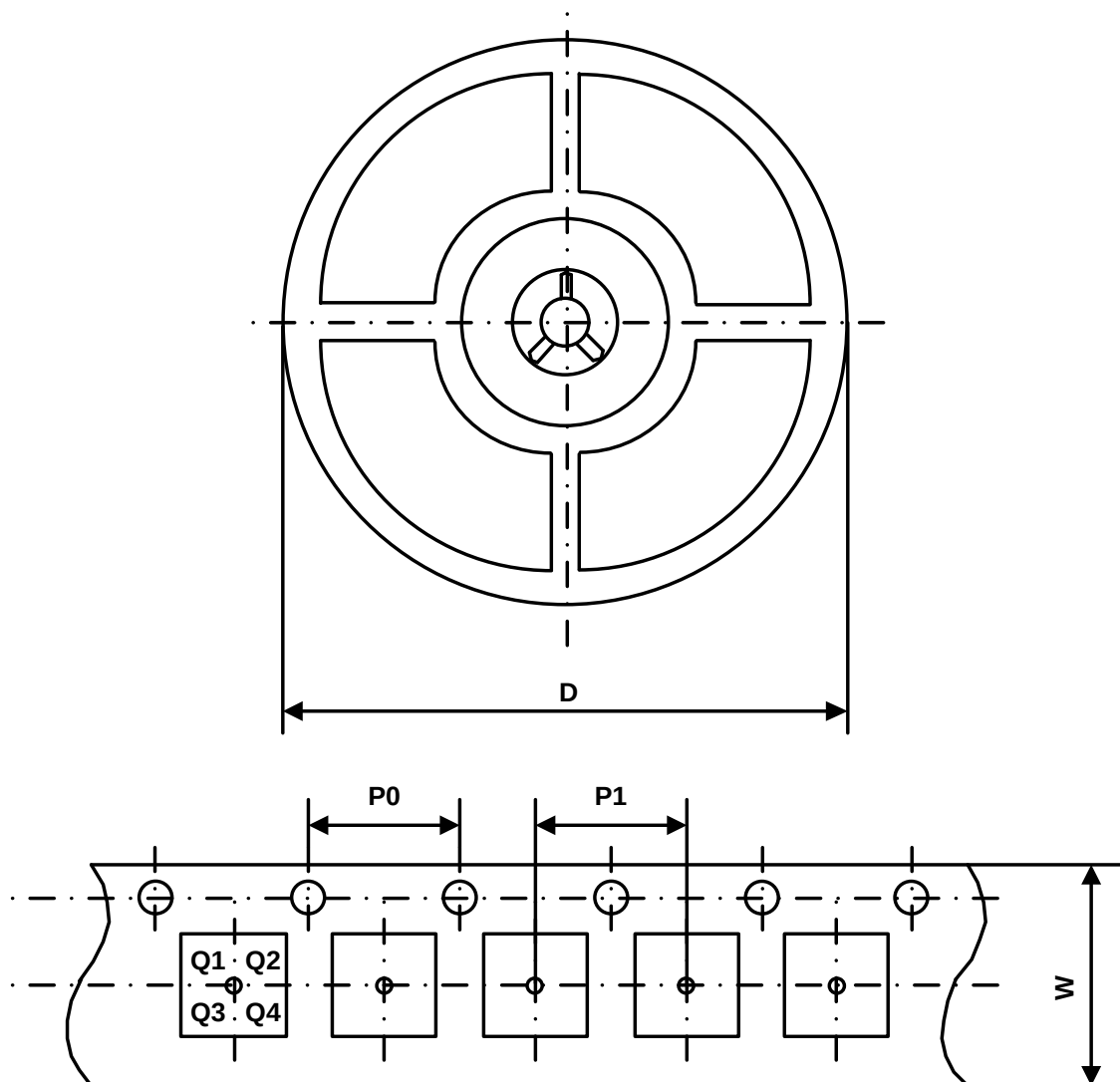
Outline Drawing



Land Pattern



12 Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM3A9606DA8	DFN8 1.4×1.0	8 mm	4 mm	4 mm	180 mm	Q1

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