3.3 V Quad LVCMOS Differential Line Receiver Translator

UM3403UG *TSSOP16*

1 Description

The UM3403UG is a quad−channel LVDS line receiver/translator offering data rates up to 400 Mbps (200MHz) and low power consumption. The UM3403UG receiver incorporates input fail−safe protection circuit that provides a known output voltage under input open−circuit and terminated (100Ω) conditions. The four independent inputs accept differential signals such as: M−LVDS, LVDS, LVPECL and HCSL and translates them to a single−ended, 3.3 V LVCMOS.

The UM3403UG also offers active high and active low enable/disable inputs (EN and $\overline{EN}$) that allow users to control outputs of all four receivers. These inputs enable or disable the receivers and switch the outputs to an active or high impedance state respectively (see Table 1). The high impedance mode feature helps to reduce the quiescent power consumption to less than 10 mW typical, when the outputs of one or more UM3403UG devices are multiplexed together.

2 Applications

- Point−to−point Data Transmission
- Backplane Receivers
- Clock Distribution Networks
- Multidrop Buses

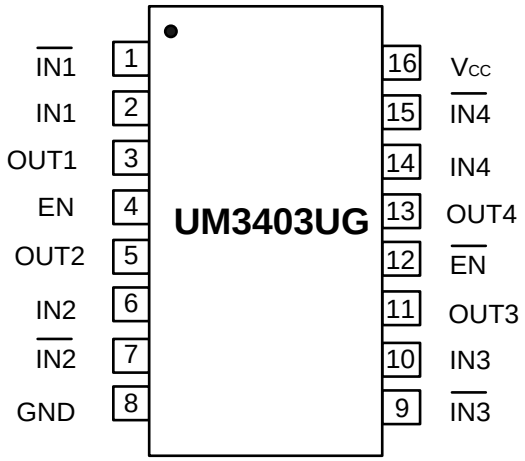
3 Features

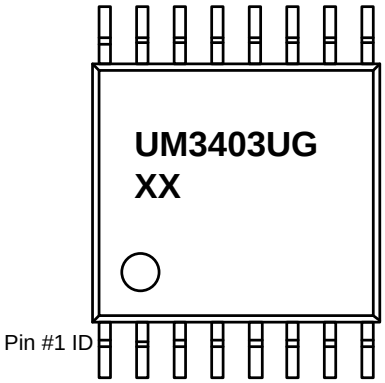
- Accepts M−LVDS, LVDS, LVPECL and HCSL Differential Input Signal Levels
- Maximum Data Rate of 400 Mbps
- Maximum Clock Frequency of 200 MHz
- 25 ps Typical Channel−to−Channel Skew
- 3.3 ns Maximum Propagation Delay
- 3.3 V ±10% Power Supply
- High Impedance Outputs When Disabled
  - Low Quiescent Power < 10 mW Typical
- Supports Open and Terminated Input Fail−safe
- −40 ℃ to +85 ℃ Ambient Operating Temperature
- 16Pin TSSOP
- These are Pb−Free Devices

4 Ordering Information

Part Number	Temp. Range	Marking Code	Package Type	Shipping Qty
UM3403UG	-40℃ to +85℃	UM3403UG	TSSOP16	3000pcs/13Inch Tape & Reel

5 Pin Configuration and Function





XX: Week Code
UM3403UG
TSSOP16

Table 5-1. Pin Functions

Number	Name	I/O Type	Description
1	$\overline{IN1}$	Input	Receiver Channel 1 Inverted Input.
2	IN1	Input	Receiver Channel 1 Non−inverted Input.
3	OUT1	LVCMOS Output	Receiver Channel 1 Output.
4	EN	Input Enable	Active High Enable. See Table 1 for output enable function.
5	OUT2	LVCMOS Output	Receiver Channel 2 Output.
6	IN2	Input	Receiver Channel 2 Non−inverted Input.
7	$\overline{IN2}$	Input	Receiver Channel 2 Inverted Input.
8	GND	Power	Power Supply Ground (Note 1)
9	$\overline{IN3}$	Input	Receiver Channel 3 Inverted Input.
10	IN3	Input	Receiver Channel 3 Non−inverted Input.
11	OUT3	LVCMOS Output	Receiver Channel 3 Output.
12	$\overline{EN}$	Inverted Input Enable	Active Low Enable. Defaults Low when left open; internal pull−down resistor. See Table 1 for output enable function.
13	OUT4	LVCMOS Output	Receiver Channel 4 Output.
14	IN4	Input	Receiver Channel 4 Non−inverted Input.
15	$\overline{IN4}$	Input	Receiver Channel 4 Inverted Input.
16	V_{CC}	Power	3.3 V ±10% Positive Supply Voltage (Note 1)

Note 1：All V_{CC} and GND pins must be externally connected to a power supply for proper operation. Bypass each supply pin with 0.01μF to GND.

6 Specifications

6.1 Absolute Maximum Ratings (Note 1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CC}	Supply Voltage Range				4.6	V
V_{IN}	Input Voltage Range		-0.5		V_{CC} +0.5	V
T_A	Operating Temperature Range		-40		85	℃
T_{STG}	Storage Temperature Range		-65		150	℃
T_L	Lead Temperature for Soldering 10 seconds				260	℃

Note 1：Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

6.2 Thermal Characteristics

Symbol	Thermal Metric	Value	Unit
θ_{JA}	Junction-to-ambient thermal resistance	73	℃/W
θ_{JC}	Junction-to-case thermal resistance	48	

6.3 Electrical Characteristics (Static)

V_{CC} = 3.3V ±10%, T_A = −40°C to +85°C. (Note1)

Symbol	Parameter		Min	Typ	Max	Unit
Power Supply						
V_{CC}	Power Supply Voltage		2.97	3.30	3.63	V
I_{CC}	No Load Supply，All Receivers Enabled (EN = V_{CC}, $\overline{EN}$ = GND, inputs open)			10	15	mA
I_{CCZ}	No Load Supply, All Receivers Disabled (EN = GND and EN = V_{CC}, inputs open)			3	5.5	mA
P_D	Power Dissipation (Note 2)				300	mW
LVCOMS Outputs						
V_{OH}	Output High Voltage	I_{OH} = −0.4 mA, V_{ID} = +200 mV	2.7	3.0		V
		I_{OH} = −0.4 mA, Input Terminated (100 Ω Across Differential Inputs)	2.7	3.0		
		I_{OH} = −0.4 mA, Input Shorted	2.7	3.0		
V_{OL}	Output Low Voltage	I_{OL} = 2 mA, V_{ID} = −200 mV	0	0.1	0.25	V
I_{OS}	Output Short Circuit Current (Note 3)	Outputs enabled, V_{OUT} = 0 V	-15	-48	-120	mA
I_{OZ}	Output Off State Current	Outputs disabled, V_{OUT} = 0 V or V_{CC}	-10	±1	+10	μA
Control Inputs （EN,$\overline{EN}$）						
V_{IH}	Input HIGH Voltage	V_{CC}= 3.3 V	2.0		V_{CC}	V
V_{IL}	Input LOW Voltage	V_{CC}= 3.3 V	0		0.8	V
I_I	Input Current	V_{IN} = 0 V or V_{CC}, Other Input = V_{CC} or 0 V	-10	±1	+10	μA
V_{CL}	Input Clamp Voltage	I_{CL} = −18 mA	-1.5	-0.9		V

6.3 Electrical Characteristics (Static)---continued

V_{CC} = 3.3V ±10%, T_A = −40°C to +85°C. (Note1)

Symbol	Parameter		Min	Typ	Max	Unit
Differential Inputs（IN,$\overline{IN}$）						
V_{CMR}	Input Common Mode Range	V_{ID} = 200 mV peak to peak; Differential Input Voltage (V_{ID}) (Notes 4 and 5) (Figure 7-2 and Figure 7-3)	0.1		2.3	V
I_{IN}	Input Current	V_{IN} = +2.8 V, V_{CC} = 3.6 V or 0 V	-25	±1	+25	μA
		V_{IN} = 0 V, V_{CC} = 3.6 V or 0 V	-30	±1	+30	
		V_{IN} = +3.63 V, V_{CC} = 0 V	-30		+30	
ESD Protection						
Symbol		**Parameter**	**Value**			**Unit**
$V_{(ESD)}$		Human Body Model	±6000			V
		Charged –Device Model	±500			V

Note 1：Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 2：Tested with 100 MHz input frequency on all channels, EN = V_{CC}, $\overline{EN}$ = GND.

Note 3：Output short−circuit current (I_{OS}) is specified as magnitude only; a minus sign indicates direction only. Note that only one output should be shorted at a time; do not exceed the maximum junction temperature specification (150 ℃).

Note 4：Guaranteed by design and characterization. Not tested in production.

Note 5：The V_{CMR} range is reduced for larger V_{ID}. Example: if V_{ID} = 400 mV, the V_{CMR} is 0.2 V to 2.2 V. A V_{ID} up to V_{CC} may be applied to the IN/$\overline{IN}$ inputs with the Common−Mode voltage set to V_{CC}/2. Propagation delay and Differential Pulse skew decrease when V_{ID} is increased from 200 mV to 400 mV. Skew specifications apply for 200 mV ≤ VI_D ≤ 800 mV over the common−mode range.

6.4 Electrical Characteristics (Dynamic)

V_{CC} = 3.3 V ±10%, T_A = −40°C to +85°C (Note 1,2)

Symbol	Parameter	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency (Note 3) All Channels Switching	200	250		MHz
$f_{DATAMAX}$	Maximum Data Rate	400			Mbps
t_{PLH}/t_{PHL}	Propagation Delay (Note 4) (Figure 7-1 and Figure 7-4)	1.8		3.3	ns
$t_{SKEW(o-o)}$	Channel−to Channel Skew (Note 5)	0	25	250	ps
$t_{SKEW(pp)}$	Part−to−Part Skew (Note 6)		50	500	ps
$t_{SKEW(p)}$	Pulse Skew $\|t_{PHL}-t_{PLH}\|$, $V_{CM} = V_{CC}/2$ (Note 7) (Figure 7-1 and Figure 7-4)	0	50	300	ps
t_r/t_f	Output Rise/Fall Time, 20% − 80% (Figure 7-1 and Figure 7-4)		600	1200	ps
$T_{jit(\varphi)}$	Additive RMS Phase Jitter Integration Range: 12 kHz to 20 MHz, f_c = 100 MHz, 25 ℃, V_{CC} = 3.3 V		161		fs
t_{PLZ}/t_{PHZ}	Output Disable Time (Figure 7-5 and Figure 7-6) R_L = 2 kΩ		10	14	ns
t_{PZL}/t_{PZH}	Output Enable Time (Figure 7-5 and Figure 7-6) R_L = 2 kΩ		2	5	ns

Note 1: Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

Note 2: Generator waveform for all tests, unless otherwise specified: f=50MHz, C_L=10pF (includes jig capacitance), t_r and t_f (10% to 90%) ≤ 2 ns for INx/$\overline{\text{INx}}$.

Note 3: f_{MAX} generator input conditions: $t_r = t_f$ < 1ns (10% to 90%), 50% duty cycle, differential (1.05V to 1.35V peak to peak). Output Criteria: 40% to 60% duty cycle, V_{OL} (max 0.4V), V_{OH} (min 2.7V), C_L = 10pF (stray plus probes)

Note 4: Measured from the differential crosspoint of the input to $V_{CC}/2$ of the output.

Note 5: $t_{SKEW(O-O)}$ is defined as skew between outputs of the same device at the same supply voltage and with equal load conditions.

Note 6: $t_{SKEW(pp)}$ is defined as skew between outputs on different devices operating at the same supply voltages and with equal load conditions. Using the same type of inputs on each device, the outputs are measured at the differential cross points.

Note 7: $t_{SKEW(p)}$ is the magnitude difference in the differential propagation delay time between the positive−going edge and the negative−going edge of the same channel.

7 Parameter Measurement Information

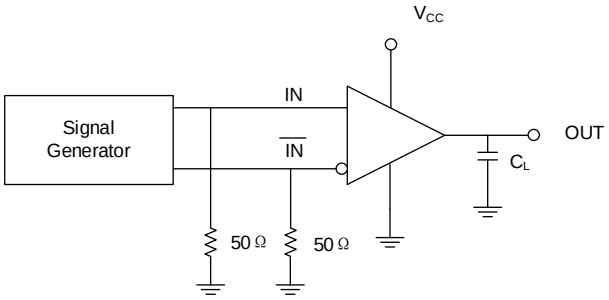


Figure 7-1. AC Reference Measurement

Note 1: C_L=Load and jig capacitance (10pF typical)

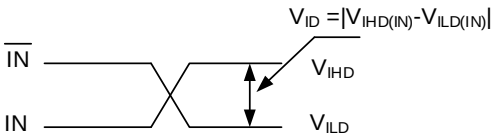


Figure 7-2. Differential Inputs Driven Differentially

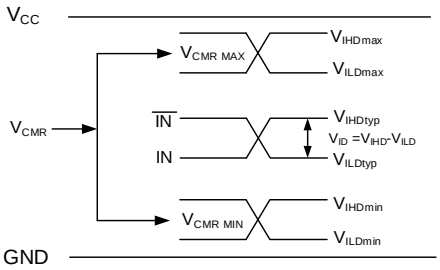


Figure 7-3. V_{CMR} Diagram

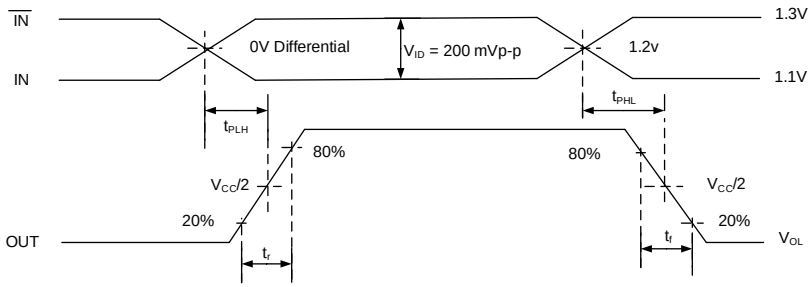


Figure 7-4. Receiver Propagation Delay, Rise and Fall Time

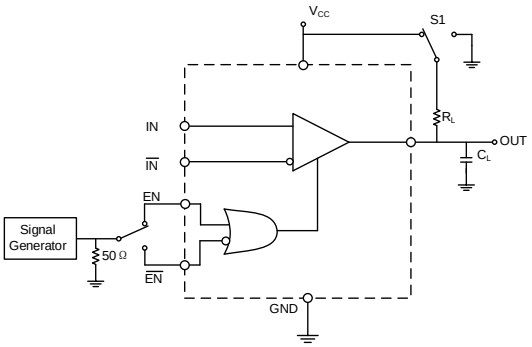


Figure 7-5. Test Circuit for Receiver Enable/Disable Delay

Note 1: C_L = Load and test jig capacitance (10 pF typical).

Note 2. S1 connected to V_{CC} for T_{PZL} and T_{PLZ} measurements.

Note 3. S1 connected to GND for T_{PZH} and T_{PHZ} measurements.

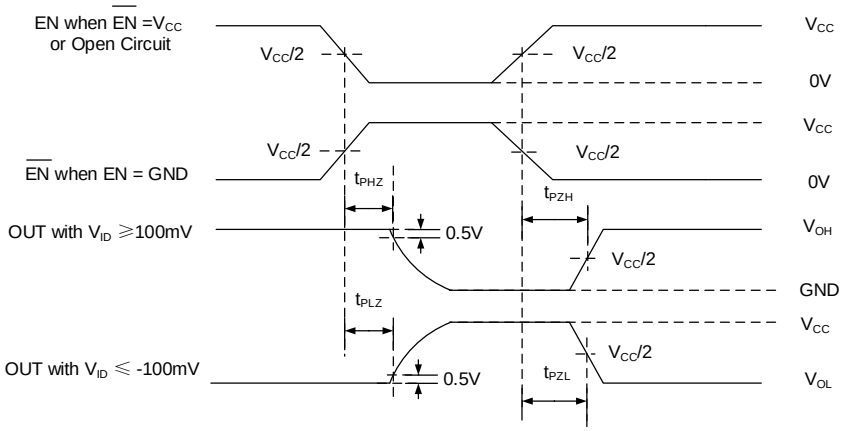


Figure 7-6. Receiver Enable/Disable Delay Waveform

8 Detailed Description

8.1 Fail−Safe Feature

The multi−level receiver's internal fail−safe circuitry is designed to provide fail−safe protection for floating/open or terminated receiver inputs, and will output a stable High−level voltage state.

8.2 Open Input Pins.

The UM3403UG is a quad receiver device, and if an application requires only 1, 2 or 3 receivers, the unused channel(s) inputs should be left OPEN. The internal input circuitry will ensure a HIGH stable output state for open inputs.

8.3 Terminated Input.

If the driver to the input is disconnected, in a TRI−STATE or power−off condition, the output will again be in a HIGH state, even with a 100Ω termination resistor across the input pins. Do not connect unused receiver inputs to ground or any other voltages.

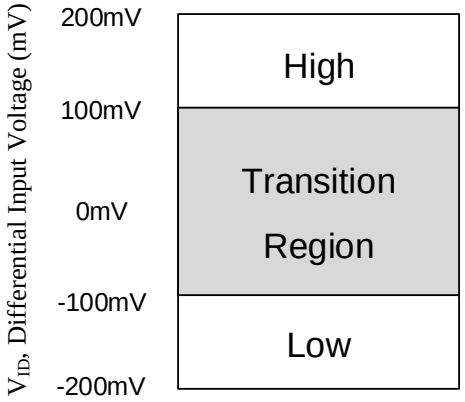


Figure 8-1. Receiver Differential Input Voltage Showing Transition Region

8.4 Output Enable Function

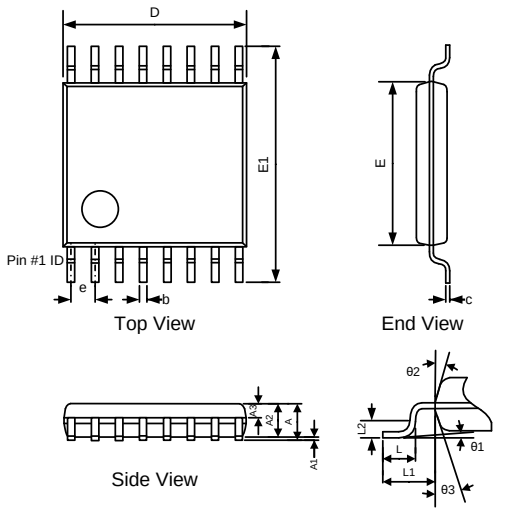
Table 8-1. Output Enable Function

Enables		Inputs	Output
EN	**$\overline{EN}$**	**IN, $\overline{IN}$**	**OUT**
L	H	X	Z
All other combinations of Enable inputs		$V_{ID} \geq 100$ mV	H
		$V_{ID} \leq -100$ mV	L
		Full Fail−safe OPEN or Terminated	H

9 Package Information

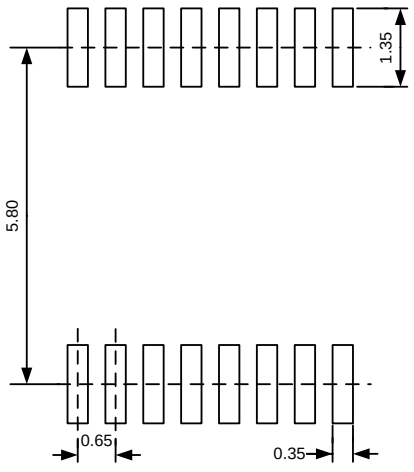
TSSOP16

Outline Drawing



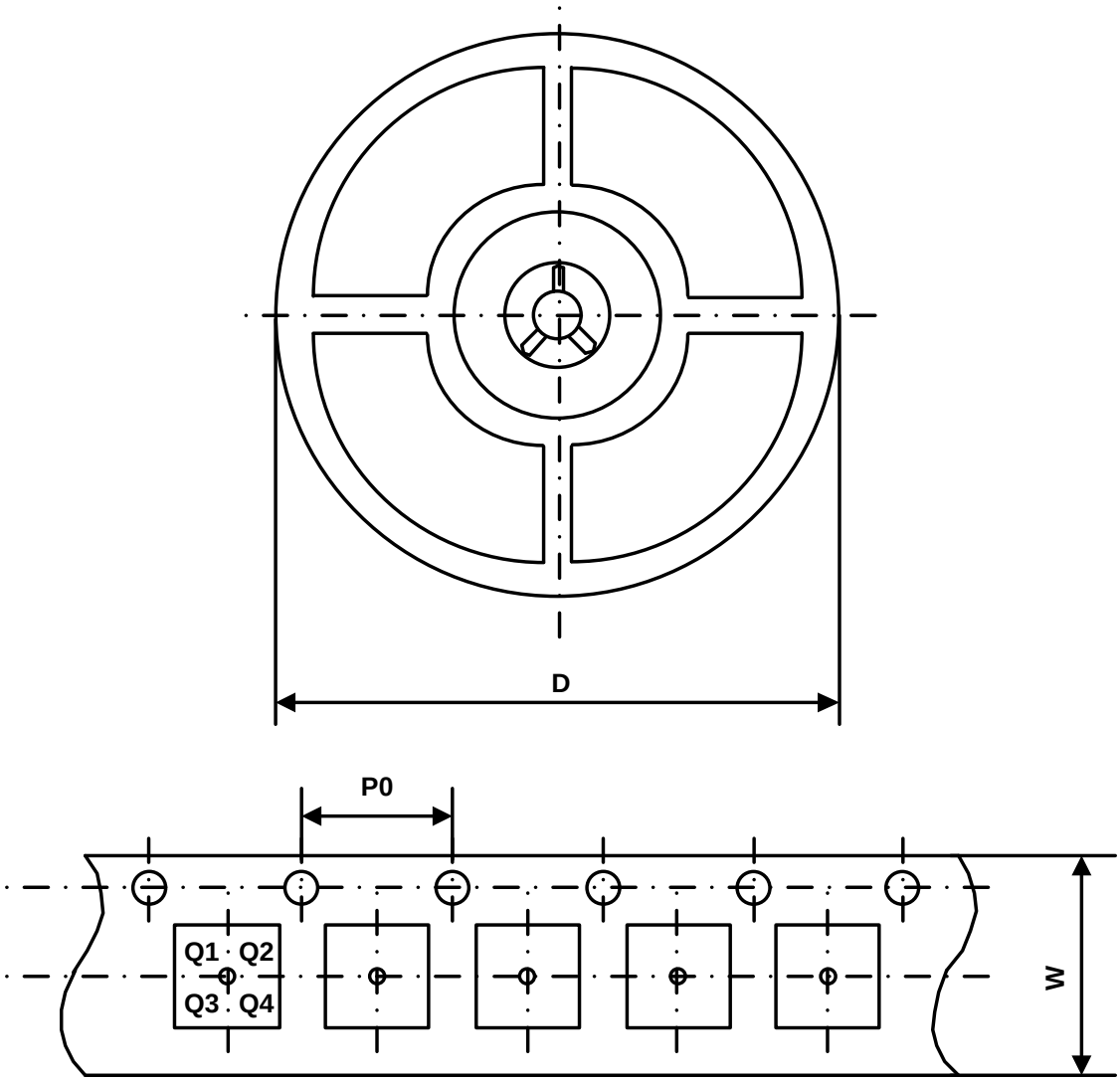
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.80	-	1.05	0.031	-	0.041
A3	0.34	0.44	0.54	0.013	0.017	0.021
b	0.19	-	0.30	0.007	-	0.012
c	0.09	-	0.20	0.004	-	0.008
D	4.86	4.96	5.10	0.191	0.195	0.201
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
L2	0.25BSC			0.010BSC		
θ1	0 °	-	8°	0°	-	8°
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°

Land Pattern



NOTES:
1. Compound dimension: 4.96×4.40.
2. Unit: mm.
3. General tolerance ±0.05mm unless otherwise specified.
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Reel Size (D)	PIN 1 Quadrant
UM3403UG	TSSOP16	16 mm	4 mm	330 mm	Q1

GREEN COMPLIANCE

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