2-Bit Bidirectional Voltage Level Translator for Open-Drain and Push-Pull Applications

UM2102S *SOT23-6*

General Description

The UM2102S allows bidirectional voltage translations between 1.5V and 5V without the use of a direction pin. The UM2102S is not a bus buffer which provides both level translation and physically isolates the capacitance to either side of the bus when both sides are connected. The UM2102S only isolates both sides when the VREF is connected to GND.

Pull-up resistors are required on both sides to provide the logic HIGH levels on the translator's bus. The size of these pull-up resistors depends on the system. The device is designed to work with Standard-mode, Fast-mode and Fast-mode Plus I^2C-bus devices in addition to SMBus devices. The maximum frequency is dependent on the RC time constant, but generally supports > 2MHz.

When the SDA1 or SDA2 port is LOW, the clamp is in the ON-state and a low resistance connection exists between the SDA1 and SDA2 ports. Assuming the higher voltage is on the SDA2 port when the SDA2 port is HIGH, the voltage on the SDA1 port is limited to the voltage set by V_{CCA}. When the SDA1 port is HIGH, the SDA2 port is pulled to the drain pull-up supply voltage (V_{CCB}) by the pull-up resistors. This functionality allows a seamless translation between higher and lower voltages selected by the user without the need for directional control. The SCL1/SCL2 channel also functions as the SDA1/SDA2 channel.

All channels have the same electrical characteristics and there is minimal deviation from one output to another in voltage or propagation delay. This is a benefit over discrete transistor voltage translation solutions, since the fabrication of the switch is symmetrical.

The translator provides excellent ESD protection to lower voltage devices, and at the same time protects less ESD-resistant devices.

Applications

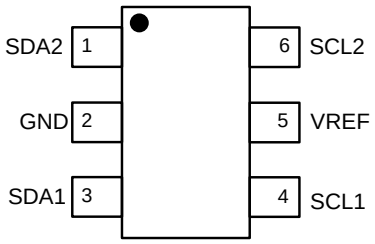
- I^2C, SMBus and SPI Level Translation
- Low-Voltage ASIC Level Translation
- Smart Card Readers
- Cell-Phone Cradles
- Portable POS Systems
- Portable Communication Devices
- Low-Cost Serial Interfaces
- Cell-Phones
- GPS
- Telecommunications Equipment

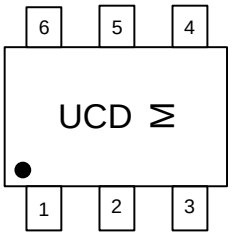
Features

- Less than 3.5ns Maximum Propagation Delay to Accommodate Standard-Mode and Fast-Mode I^2C-Bus Devices and Multiple Masters
- Open-Drain I^2C-Bus I/O Ports (SCL1, SDA1, SCL2 and SDA2)
  Provides Bidirectional Voltage Translation with no Direction Pin
- Low 3.0Ω ON-State Connection between Input and Output Ports Provides Less Signal Distortion
- 5V Tolerant I^2C-Bus I/O Ports to Support Mixed-Mode Signal Operation
- Lock-up Free Operation
- Flow through Pinout for Ease of Printed-Circuit Board Trace Routing
- ESD Protection :
  Exceeds 2000V HBM per JESD22-A114
  200V MM per JESD22-A115
  1000V CDM per JESD22-C101
- Package Offered: SOT23-6

Pin Configurations Top View

(Top View)





M: Month Code
UM2102S
SOT23-6

Pin Description

Pin Number	Name	Function
1,6	SDA2,SCL2	High-voltage side; connected to V_{CCB} through a pull-up resistor
2	GND	Ground(0V)
3,4	SDA1,SCL1	Low-voltage side; connected to V_{CCA} through a pull-up resistor
5	V_{REF}	Connected to V_{CCA} to enable the chip and connected to GND to isolate the bus

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM2102S	SOT23-6	UCD	3000pcs/7Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{REF}	Reference Voltage		-0.5 to +6	V
V_I	Input Voltage		-0.5 (Note 2) to +6	V
$V_{I/O}$	Voltage on an Input/Output Pin		-0.5 (Note 2) to +6	V
I_{ch}	Channel Current (DC)		+128	mA
I_{IK}	Input Clamp Current	V_I＜0V	-50	mA
T_{stg}	Storage Temperature Range		-65 to +150	℃

Note 1: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note 2: The input and input/output negative voltage ratings may be exceeded if the input and input/output clamp current ratings are observed.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{I/O}$	Voltage on an Input/ Output Pin	SCL1, SDA1, SCL2, SDA2	0	5	V
V_{REF} (Note 3)	Reference Voltage		0	3.6	V
$I_{sw(pass)}$	Pass Switch Current			64	mA
T_{amb}	Ambient Temperature	Operating in Free-Air	-40	+85	℃

Note 3: V_{REF} (V_{CCA})≤V_{CCB} −1 V for best results in level shifting applications.

Electrical Characteristics

T_{amb}=−40°C to +85°C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ (Note 4)	Max	Unit
V_{IK}	Input Clamping Voltage	I_I=−18mA; V_{REF}=0V				-1.2	V
I_{IH}	HIGH-Level Input Current	V_I=5V; V_{REF}=0V				5	μA
$C_{io(off)}$	Off-State Input/Output Capacitance	SCLn, SDAn; V_O=0V or 3V;V_{REF}=0V			10	12.2	pF
$C_{io(on)}$	On-State Input/Output Capacitance	SCLn, SDAn; V_O=0V or 3V;V_{REF}=3V			8	12	pF
R_{on}	ON-State Resistance (Note 5)	SCLn, SDAn; (Note 6) V_I=0; I_O=64mA	V_{REF}=4.5V		2.0	5.0	Ω
			V_{REF}=3V		2.4	6.0	
			V_{REF}=2.3V		3.1	8.0	
			V_{REF}=1.5V		11	32	
		SCLn, SDAn; V_I=2.4V; I_O=15mA	V_{REF}=4.5V		4.6	7.5	
			V_{REF}=3V		50	80	
		SCLn, SDAn; V_I=1.7V; I_O=15mA	V_{REF}=2.3V		50	80	

Note 4：All typical values are at T_{amb}=25°C.

Note 5：Measured by the voltage drop between the SCL1 and SCL2, or SDA1 and SDA2 terminals at the indicated current through the switch.
ON-state resistance is determined by the lowest voltage of the two terminals.

Note 6：Guaranteed by design.

Switching Characteristics (Translating Down)

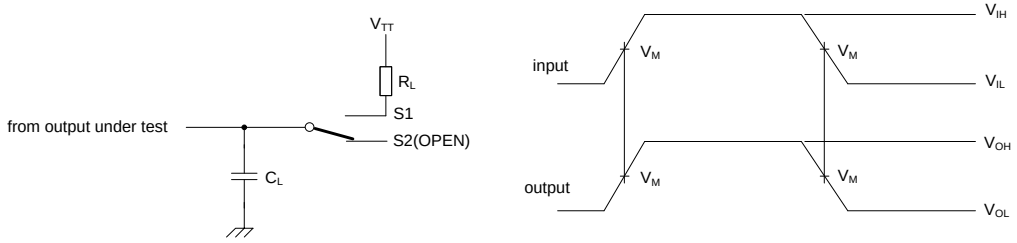
Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Min	Max	Min	Max	Min	Max	
V_{REF} = 2.3V; V_{IH} = 3.3V; V_{IL} = 0V; V_M =1.15V(see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1.	0	2.5	0	1.7	0	1.2	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	2.5	0	2.0	0	1.3	ns
V_{REF} =1.5V; V_{IH} = 2.5V; V_{IL} = 0V; V_M = 0.75V (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL2 or SDA2 to (Output) SCL1 or SDA1.	0	2.5	0	1.7	0	1.2	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.0	0	2.0	0	1.3	ns

Switching Characteristics (Translating Up)

Over recommended operating free-air temperature range (unless otherwise noted). Values guaranteed by design.

Symbol	Parameter	Test Conditions	C_L=50pF		C_L=30pF		C_L=15pF		Unit
			Min	Max	Min	Max	Min	Max	
V_{REF} = 2.3V; V_{IH} = 2.3V; V_{IL} = 0V; V_{TI} = 3.3V; V_M =1.15V ; R_L =300 Ω (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2.	0	2.35	0	1.5	0	1.0	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.35	0	2.25	0	1.4	ns
V_{REF} =1.5V; V_{IH} = 1.5V; V_{IL} = 0V; V_{TI} = 2.5V; V_M = 0.75V ; R_L =300 Ω (see Figure 1).									
t_{PLH}	LOW to HIGH Propagation Delay	from (Input) SCL1 or SDA1 to (Output) SCL2 or SDA2.	0	2.35	0	1.5	0	1.0	ns
t_{PHL}	HIGH to LOW Propagation Delay		0	3.5	0	2.5	0	1.5	ns

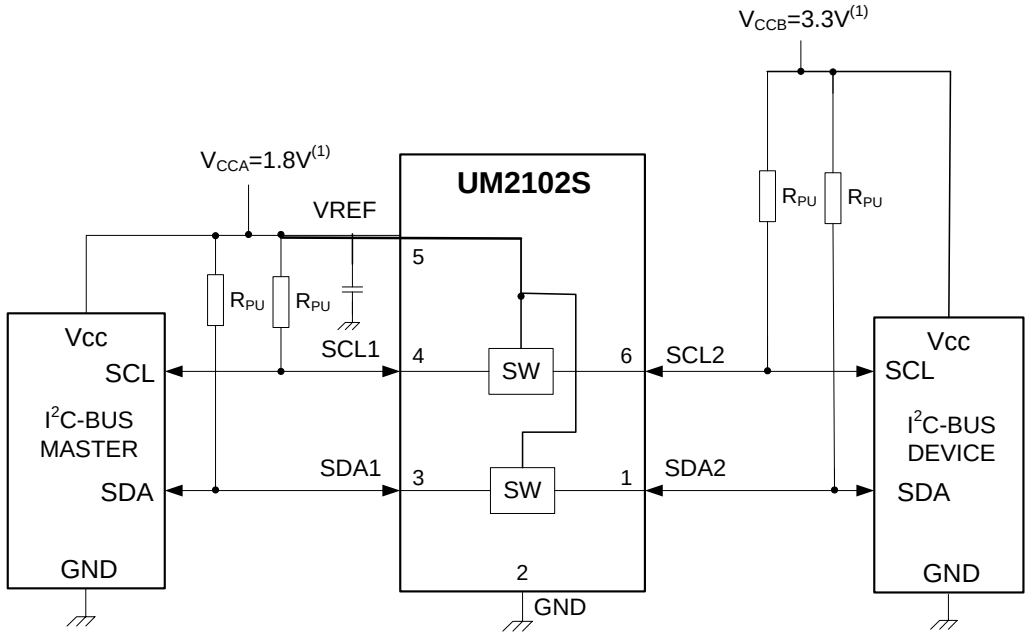


a. Load circuit **b. Timing diagram; high-impedance scope probe used**

S1 = translating up; S2 = translating down.
C_L includes probe and jig capacitance.
All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz; Z_o = 50 Ω; t_r ≤ 5 ns; t_f ≤ 5 ns.
The outputs are measured one at a time, with one transition per measurement.

Fig 1. Load circuit for outputs

Typical Application Circuit



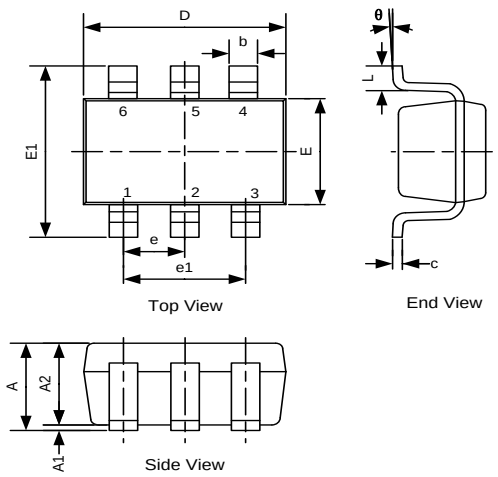
(1) The applied voltages at V_{CCA} and V_{CCB} should be such that V_{CCB} is at least 1 V higher than V_{CCA} for best translator operation.

Figure 2. Typical application circuit (switch always enabled)

Package Information

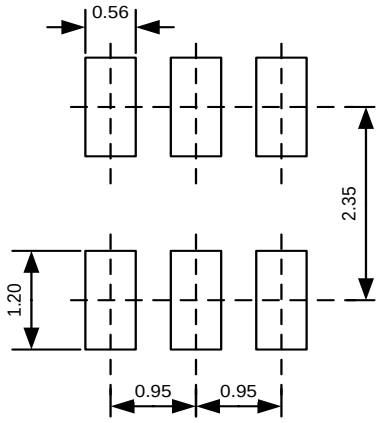
SOT23-6

Outline Drawing



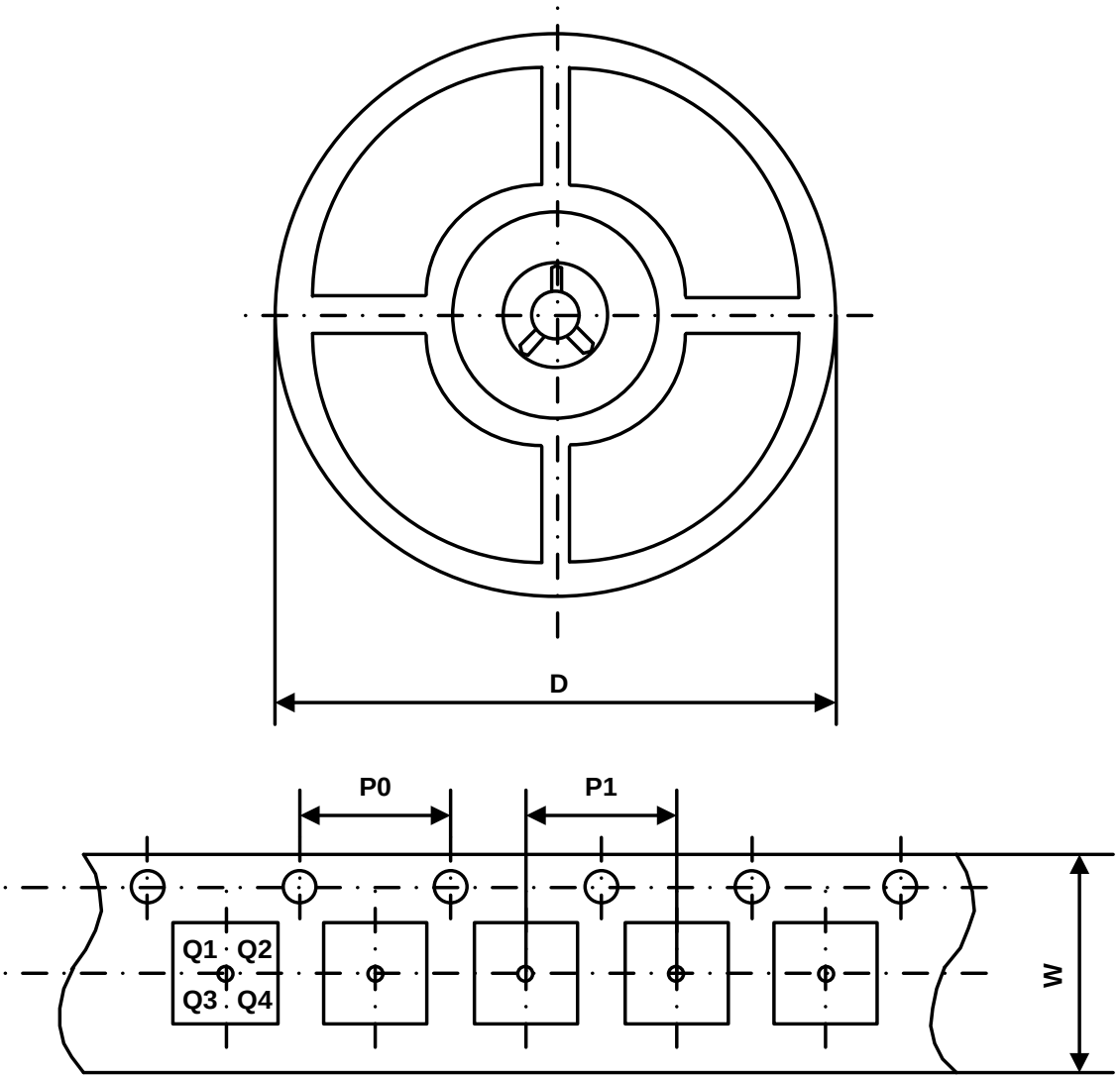
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.013	1.15	1.40	0.040	0.045	0.055
A1	0.00	0.05	0.10	0.000	0.002	0.004
A2	1.00	1.10	1.30	0.039	0.043	0.051
b	0.30	-	0.50	0.012	-	0.020
c	0.10	0.15	0.20	0.004	0.006	0.008
D	2.82	-	3.10	0.111	-	0.122
E	1.50	1.60	1.70	0.059	0.063	0.067
E1	2.60	2.80	3.00	0.102	0.110	0.118
e	0.95REF			0.037REF		
e1	1.90REF			0.075REF		
L	0.30	-	0.60	0.012	-	0.024
θ	0 °	-	8 °	0 °	-	8 °

Land Pattern



NOTES:
1. Compound dimension: 2.92×1.60;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Packing Information



Part Number	Package Type	Carrier Width (W)	Pitch (P0)	Pitch (P1)	Reel Size (D)	PIN 1 Quadrant
UM2102S	SOT23-6	8 mm	4 mm	4 mm	180 mm	Q3

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