

Portable Systems Demand Proper ESD Protection

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Portable product designers are constantly challenged to make smaller devices with increased functionality. Doing so calls for more complex semiconductors, requiring submicron processes. In turn, these semiconductors become increasingly more sensitive to the effects of electrostatic discharge (ESD). Portable systems are constantly exposed to ESD. An unsuspecting user can inject a hazardous charge during normal device operation, and then perceive the resulting system failure as poor product quality. Moreover, products shipped into Europe must meet strict ESD immunity standards or risk being banned. Increased device sensitivity coupled with increasingly miniaturized form factors have increased the challenge of designing adequate ESD protection. It requires a combination of good board layout and state-of-the-art protection components to properly complete the task.

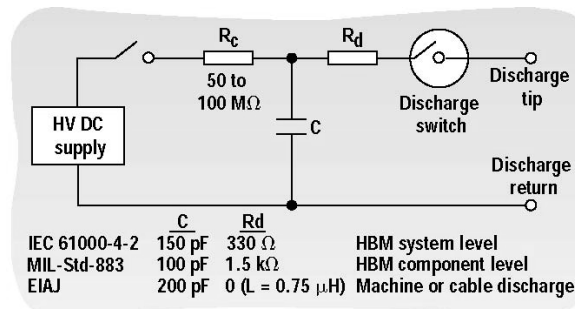
ESD is the result of a sudden redistribution of electrons between two objects. The contact and separation of two nonconductive materials causes a transfer of electrons between the objects, thereby creating an excess charge on each. When brought into close proximity of a conducting material, the result is a high-voltage discharge into the conductive object (an ESD event). Certain materials will tend to lose charge, while others will gain charge. The tendency of a material to gain or lose charge is given by the triboelectric series. The human body is one of the most common generators of ESD. Even as a person goes through their daily routine, the contact and separation of the soles of their shoes leads to a buildup of static charge on a person's body. The magnitude of the charge will only be a few micro Coulombs, but the voltage potential with respect to earth ground can exceed several thousand volts. It is very common for a person to develop voltages in excess of 15 kV. Discharge occurs when a person comes in contact with a conductive object such as a metal doorknob or a cellular telephone's input/output (I/O) port. Damage or destruction of semiconductors may occur as a result of the high static potential of the ESD event, or as a result of the discharge current. Tests have shown that devices may fail after one very high discharge or due to the cumulative effects of several discharges of lower potential.

ESD damage can be divided into three categories:

Catastrophic, with permanent damage to the device from junction shorting, oxide punch-through, or metallization melting.

Latch-Up, with temporary malfunction resulting in device upset or data loss.

Latent, where damaged devices may continue to operate, but will degrade over time, eventually failing.



1. This simple schematic circuit can be used to simulate ESD.

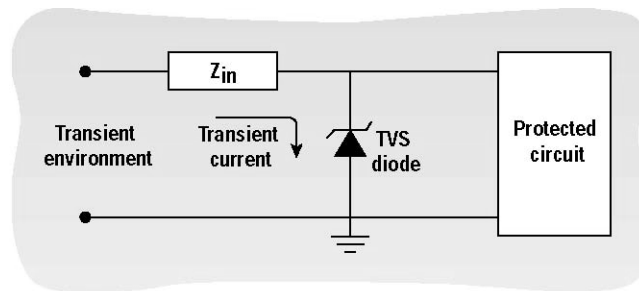
Latent ESD damage is subtle and difficult to identify through failure analysis. The end product maybe perceived as being of poor quality by the end user.

Several models exist to simulate the ESD event. Each is designed to describe the threat in a real-world environment. The discharge model is typically a voltage source feeding a resistor/capacitor network. Resistor and capacitor values vary depending upon the standard. For example, one of the most widely used standards is MIL-STD-883, Method 3015 (also formalized as ANSI/EOS/ESD-S5.1 1993). It is designed to describe the "human-body model" ESD threat at the component level. In this standard, a 100pF capacitor is charged to a

specified test voltage and discharged into a component's pin through a 1.5k resistor with another pin serving as the return path. While the capacitor may be charged to a few thousand volts, the 1.5k resistor will largely limit the peak discharge current. The component is checked for damage after three (each) positive and negative pulses. This is typically the test that semiconductor manufacturers will perform to test the ESD sensitivity of their component. A second, less popular model is the charged-device model (CDM). This model simulates the printed-circuit-board (PCB) assembly and test-handler environment. Essentially, a component may become charged as it slides down a rail to a tester. When the charged component comes into contact with a metallic surface, it will discharge into the surface and potentially damage the device.

ESD STANDARDS

Standard IEC61000-4-2 is probably the most important ESD standard for designers to take into consideration. This is because it is a system-level test that equipment must pass before being allowed into the European marketplace. Additionally, IEC61000-4-2 has become the most widely accepted ESD immunity standard in several countries. Similar to ANSI/EOS/ESD-S5.1-1993, IEC61000-4-2 models human-body ESD. The test is performed by discharging a 150-pF capacitor through a 330- resistor. The peak current achieved is five times greater than that of ANSI/EOS/ESD-S5.1-1993. This is one reason why devices may fail at the system level even though they pass the component-level test. Discharge into the equipment may be through direct contact (contact discharge) or just prior to contact (air discharge). Standard IEC 61000-4-2 divides the ESD into four threat levels. Test voltages at the threat levels range from 2 to 15 kV with peak discharge currents up to 30 A. The ESD waveform as defined by IEC 61000-4-2 reaches peak magnitude in approximately 1 ns and has a total duration of only 60 ns. While the ESD pulse contains little energy, the resulting effect can be devastating to sensitive semiconductor devices. Sensitive points of the equipment are to be tested with a combination of positive and negative discharges. Sensitive areas of a cell phone, for example, would include I/O ports, battery contacts, light-emitting-diode (LED) displays, antenna, and keyboard.



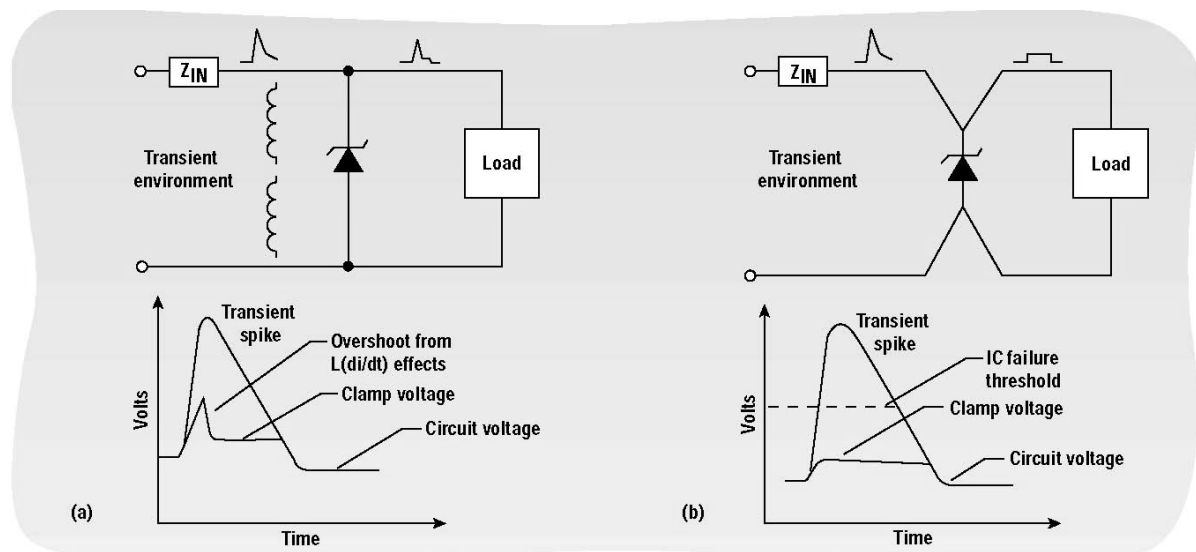
2. The operation of a TVS diode serves to protect a variety active devices from ESD damage.

ESD PROTECTION

Some form of ESD protection is a necessary part of good system design. All user-accessible areas are prone to static discharge. Especially vulnerable are keyboards, data, and I/O ports. To guard against externally radiated ESD emissions, shielding of equipment cases and cables as well as good bonding practices are required. External components designed to absorb transient energy are normally necessary to protect systems from conducted transient events. Although several types of transient-suppression devices are available, few have been optimized for suppression of ESD. A poorly chosen device will not only be ineffective, but could interfere with the normal operation of the protected circuit. The suppression component must limit the voltage across the protected device to a level just above the normal operating voltage, but well below the destructive threshold (**Fig. 1**). In addition to low operating and clamping voltage, the suppression element should also have the following characteristics:

- Extremely fast response time.
- Capacity to handle high peak-transient currents.
- Capability to remain undamaged by repetitive ESD strikes.
- Minimal size.
- Low-reverse leakage current.

While other technologies boast several of the characteristics previously outlined, transient-voltage-suppression (TVS) diodes meet all of the listed criteria and offer the lowest clamping voltage of any other suppression technology. TVS diodes are solid-state devices specifically designed to protect sensitive semiconductors from the damaging effects of transient voltages. TVS diodes can protect metal-oxide-semiconductor (MOS), complementary-MOS (CMOS), bipolar, transistor-transistor logic (TTL), and gallium-arsenide (GaAs) devices. For data and supply voltages down to +5 VDC, a device employing a p-n junction construction is used. The transient-power and transient-current capability of the TVS diode is proportional to the junction area. TVS diodes are constructed with large cross-sectional-area junctions for handling the high transient currents associated with ESD events. For circuits operating below +5 VDC, high leakage currents and junction capacitance render conventional p-n junction technology impractical. Recent innovations in TVS-diode design are providing devices capable of protecting circuits operating at below +5 VDC, while adding minimal leakage current and capacitance. The best strategy for dealing with transient events is to divert the transient current away from the sensitive semiconductor components. TVS diodes are shunt-connected across the protected line (Fig. 2). When a transient voltage exceeds the normal operating voltage of the line, the TVS diode-junction avalanches providing a low impedance path for the transient current. As a result, the transient current is diverted away from the protected circuit and shunted through the TVS diode. The voltage across the protected circuit is limited to the clamping voltage of the TVS diode. The device automatically returns to a high impedance state after the transient event passes. TVS diodes will not wear out or degrade as long as they are operated within specified limits. Transient protection for portable systems is recommended on the circuit board where there is a conductive path to the outside world.



3. The effects of parasitic inductance can be minimized by keeping shunt signal paths as short as possible.

TVS diodes are available in a wide variety of small surface-mount packages that are suitable for use in portable systems. Multiline arrays are available in tiny SC70 packages that take up less than 4.8 mm^2 of PCB space. In situations where routing does not support the use of arrays or only one line needs to be protected, single-line components in SOD-323 packages may be used. Still other devices combine resistors and capacitors for electromagnetic-interference (EMI)/RF-interference (RFI) filtering or termination, with TVS diodes for ESD protection. While many combinations and choices exist for TVS diodes, the quality and electrical characteristics vary among different manufacturers. The designer must consider device ratings and performance or the chosen "solution" may not provide adequate protection. First, the TVS diode should be rated to handle a minimum of 8-kV (contact) and 15-kV (air) ESD surges per IEC 61000-4-2 without damage. Many manufacturers have inhouse requirements that exceed these ratings. One of the most important considerations is the device-clamping voltage. The clamping voltage is the voltage across the TVS during the ESD event. Consequently, this is the stress voltage affecting the protected IC. The susceptibility of gate oxides to ESD damage increases as oxide layers become thinner with advanced process technology. This means that the higher clamping voltage will produce more stress on the protected device and increase the probability of failure. TVS arrays with the same pin configuration, and

package can have vastly different clamping voltages.

The sophistication of today's electronics means that schemes such as "general" protection devices, switching diodes, spark gaps, or other methods can no longer be used. For example, consider the universal-serial-bus (USB) interface standard. Since it is designed as a hot insertion and removal interface for computers and peripherals, exposed USB connectors are highly susceptible to ESD discharges. State-of-the-art CMOS processes are used to manufacture USB integrated circuits (ICs). Their fine geometry makes them extremely sensitive to the high static voltages associated with ESD events. Protecting a USB port from damage can be difficult. Since USB is a high-speed connection, the loading capacitance of the protection device must be minimized. Also, in order to achieve optimum protection, the suppression device should operate as close to the normal operating voltage of the circuit as possible. In the case of USB, the operating voltage should be +5 VDC. Finally, both data and power ports are exposed in the USB connector and should be protected. New products combine the termination and EMI-filtering requirements of the USB specification with ESD protection in small SOT-23 packages. These devices can replace nine or more discrete components.

PCB LAYOUT

PCB layout is an important part of transient-immunity design. This is especially critical in portable systems where the threat of ESD exists. Parasitic inductance in the protection path can result in significant voltage overshoot and may exceed the damage threshold of the protected IC. This is especially critical in the case of fast rise-time transients such as ESD. Recall that the voltage developed across an inductive load is proportional to the time rate of change in current ($V = L di/dt$). An ESD-induced transient reaches a peak in less than 1 ns (per IEC 1000-4-2). Assuming a trace inductance of 20 nH/in. and a quarter-inch trace, the voltage overshoot will be +50 VDC for a 10-A pulse. The primary rule of thumb is to minimize the effects of parasitic inductance by making the shunt paths as short as possible (**Fig. 3**). All inductive paths must be considered, including the ground return path, the path between the TVS and the protected line, and the path from the connector to the TVS device. Also, The TVS device should be placed as close to the connector as possible to reduce transient coupling into nearby traces. The secondary effects of radiated emissions can cause upset to other areas of the board even if there is no direct path to the connector. Long signal traces will act as antennas to receive energy from fields produced by the ESD pulse. By keeping line lengths as short as possible, the efficiency of the line to act as an antenna for ESD-related fields is reduced. One should minimize interconnecting line lengths by placing devices with the most interconnects as close together as possible. Finally, avoid running critical signal lines near board edges or next to protected lines.



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