

ESD Protection for High Speed I/O Data Lines

Abstract

These days, our modern society has rapidly come to fully depend on electronics. And modern computers are based increasingly on low power logic chips, all with ESD sensitivity due to MOS dielectric breakdowns and bipolar reverse junction current limits. The ICs that control I/O ports (USB, Ethernet, etc.) are not an exception since the majority of them are designed and manufactured based on CMOS processes which make them extremely sensitive to damage from ESD conditions. Because the majority of I/O ports are hot insertion and removal systems, they are extremely vulnerable to receive ESD conditions possibly generated by the users or by air discharges. Users can induce ESD conditions while plugging or unplugging any cables, and air discharges can happen a few inches away from the conducting surface.

What ESD (ElectroStatic Discharge) can cause are catastrophic damage to I/O ports, IC malfunction, and worst of all, ghost data bits in electronic systems. When product damage or product malfunction results in a “Hard failure” or destroyed component, it is easy to isolate and replace the failed component and put the system back in service, however, if a “soft failure” occurs (CMOS component degraded), the system anomaly is not detected in retesting, and hours are wasted in troubleshooting because the system continues to produce irregular data bits. Such failures have a very negative impact in the final product because they increase the cost of warranty repairs and diminish the perception of the product’s quality.

In addition to all the previous problems caused by static discharge conditions in unprotected ICs, ESD protection now is becoming a strong requirement mainly in the European market, which causes the manufacturers to be barred from selling in this market unless their product/equipment meets the minimum levels of ESD performance.

Electrostatic Discharge Generation

When two insulating materials are rubbed together, an electric charge builds up between them (as electrons are stripped off one surface and deposited on the other surface). The surface with the excess of electrons becomes negatively charged, and the surface with the shortage of electrons becomes positively charged. This effect is known as the “triboelectric” effect (the action of rubbing). Electrostatic voltage is then a function of the separation of the materials in the series, the intimacy of contact, and the rate of separation. Therefore, any time there are two nonconductive materials flowing in opposition to each other, an electrostatic voltage will be generated. The level of electrostatic potential generated depends on the relative charge affinity between materials, the humidity, and other factors.

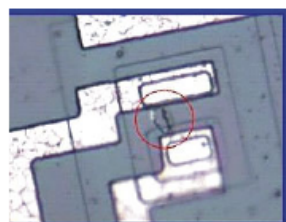
As shown in the Figure below, an ESD event can easily destroy an IC in several ways, resulting in one or more of these problems:

- junction leakage
- short circuits or burn-out
- dielectric rupture
- resistor-metal interface rupture
- resistor-metal fusing

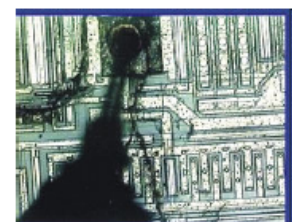
Soft errors requiring shutdown and restart can be induced by ESD strike in the same time.



Oxide fusing point



Metallic junction damage



Metallization damage

Through time, industrial standards have been developed to standardize the ESD compliance of semiconductor devices, some of the most common standards are described below:

IEC 61000-4-2: This International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects.

IEC 61000-4-5: This International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to Lighting conditions (surge 8 x 20µs).

ESD Protection for High Speed I/O Data Lines

Protection for ESD requires engineers and designers to add external protection devices or select robust ICs with a certain level of protection built in. Having ICs with some sort of protection built in sometimes is not entirely convenient since the ICs must absorb the power created by the ESD conditions which may cause problems in the IC's functionality or reduce its efficiency. Therefore, external protection devices are the ideal case to keep the ESD conditions and their secondary effects away from the ICs. ESD protection for high speed I/O data lines not only implicates compliance with the ESD industrial standards previously explained, but it also implicates the usage of very sophisticated devices capable to operate under conditions of high speed data transmission and the high technology of the IC controllers, so conventional methods using discrete devices would be obsolete and non-efficient to protect high speed I/O data lines. Some of the key characteristics that ESD protection devices intended for high speed I/O data lines must have are listed below:

- Low capacitance (<5.0 pf) to minimize the signal attenuation at high speed data rate (such as 480Mbps for USB 2.0)
- Fast time operation response (nanosecond) to protect the ICs against the fast rise time of the ESD pulses
- Low leakage current to minimize the power consumption under normal operation conditions
- Robustness to drive and absorb repetitive ESD conditions without damage
- Integrated and reduced package

For multi-line protection devices it is also vitally important for all line protection circuits to have symmetrical characteristics.

Union Device UM5204EEXF

Union Semiconductor has developed a unique Low Capacitance TVS Diode Array (UM5204EEXF) designed to protect sensitive electronics such as communications systems, computers, and computer peripherals against damage due to ESD conditions or transient voltage conditions. Because of its very low capacitance array configuration, it can be used in high speed I/O data lines .

The integrated design of the UM5204EEXF offers surge rated, low capacitance steering diodes and a TVS diode integrated in a single package (SOT23-6). If a transient condition occurs, the steering diodes will drive the transient condition either to the positive polarity of the power supply or to ground. The TVS device protects the power line against over-voltage conditions to avoid damage in any downstream components. In addition to its low capacitance characteristics, the UM5204EEXF from Union Semiconductor complies with the most common industrial standards for ESD Protection: IEC61000-4-2, and IEC61000-4-5.

The following figure shows the UM5204EEXF device's configuration and the equivalent circuit.

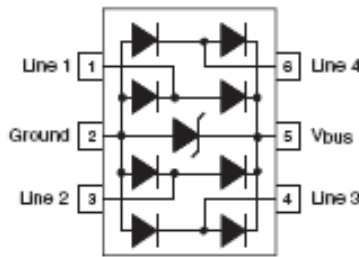


Figure 1

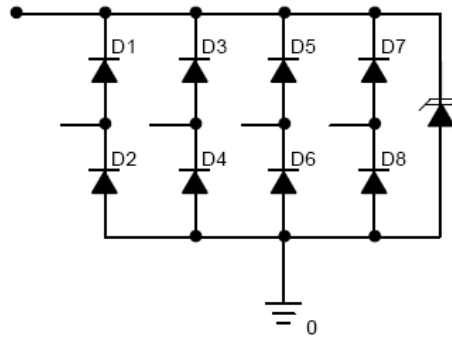


Figure 2

DC Parameters

As previously mentioned, one of the most important characteristics that any device intended to be used for ESD protection in high data I/O lines is to have low leakage current to minimize the power consumption of the system. The UM5204EEXF device actually offers very low values of leakage current which make them fully useful for high data I/O lines.

Capacitance Between I/O Lines and Between I/O Lines and Ground

As previously mentioned, “low capacitance (<5.0 pf)” is one of the most important characteristics that any device intended to be used in high data I/O lines must have in order to minimize the signal attenuation at high speed data rate. This characteristic is critical, otherwise, the functionality of the system could be affected dramatically during high speed operation.

Since the UM5204EEXF is a low capacitance (<2.0 pf between I/O lines and ground; <1.0 pf between I/O lines) TVS diode array, it can be used either in USB 2.0 or USB 1.1 components.

Compliance with IEC 61000–4–2, ESD International Standard

IEC 61000–4–2, 8.0 KV (Contact)
IEC 61000–4–2, 15 KV (Air)

The IEC61000–4–2 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to static electricity discharges, from operators directly, and to adjacent objects.

It additionally defines ranges of test levels which relate to different environmental and installation conditions and establishes test procedures. The object of this standard is to establish a common and reproducible basis for evaluating the performance of electrical and electronic equipment when subjected to electrostatic discharges. In addition, it includes electrostatic discharges which may occur from personnel to objects near vital equipment.

The IEC61000–4–2 specification defines the preferential range of test levels for the ESD test which is described in Table 2.

Table 2. Test Levels

1a – Contact Discharge		1b – Air Discharge	
Level	Test Voltage (KV)	Level	Test Voltage (KV)
1	2.0	1	2.0
2	4.0	2	4.0
3	6.0	3	8.0
4	8.0	4	15
X	special	X	special

* “X” is an open level. The level has to be specified in the dedicated equipment specification. If higher voltages than those shown are specified, special test equipment may be needed.

The IEC61000–4–2 specification also defines what should be the characteristics and performance of the ESD generator, these characteristics are listed below.

Specifications

- Energy Storage Capacitance ($C_s + C_d$): $150 \text{ pF} \pm 10\%$
- Discharge Resistance (R_d): $330 \text{ Ohms} \pm 10\%$
- Charging Resistance (R_c): between 50Mohms and 100Mohms
- Output Voltage (see Note 1): up to 8.0kV (nominal) for contact discharge; up to 15kV (nominal) for air discharge

NOTE:

1. Open circuit voltage measured at the energy storage capacitor.

Figure 3 illustrates the simplified diagram of the ESD generator. Figure 4 illustrates the typical waveform of the ESD generator (information taken from the IEC61000–4–2 spec):

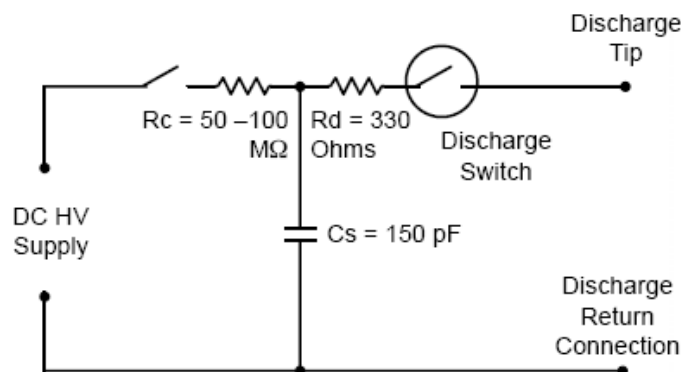


Figure3 . ESD Generator, Simplified Diagram

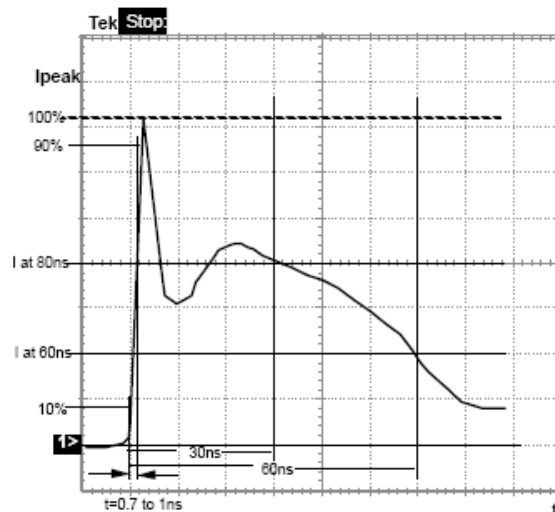


Figure 4. Typical Output's Waveform of the ESD Generator

The equipment used for these ESD tests is shown in Figure 5. Figure 6 shows an oscilloscope plot that illustrates a real waveform sample taken from the output of this ESD generator.



Figure 5. ESD Generator, NoiseKen ESS-2000

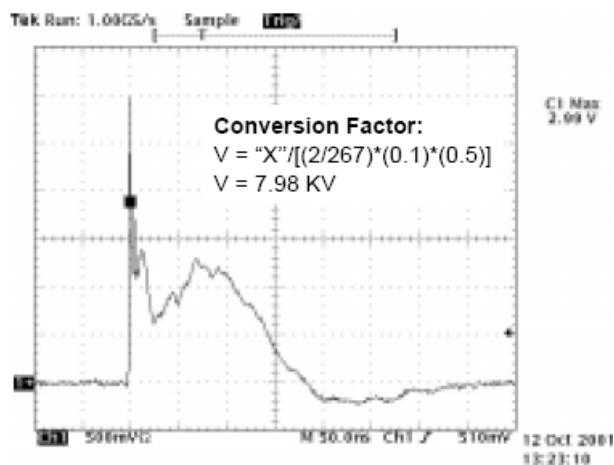


Figure 6 . Real Waveform Sample Taken from ESD Generator

Some UM5204EEXF devices were tested under the contact and 15 kV air) and the results observed are listed in Table 3.

Table 3. ESD Characterization Results

IEC Rating (10P) IEC 61000-4-2	Contact		Air	
	Serial Number	Pass/ Fail	Serial Number	Pass/ Fail
8.0 KV	1	P		
8.0 KV	2	P		
8.0 KV	3	P		
15 KV			4	P
15 KV			5	P
15 KV			6	P

NOTE: All the devices characterized under the IEC61000-4-2 conditions passed the test.

Compliance with IEC 61000-4-5, Lighting International Standard

IEC 61000-4-5 (Surge 8 x 20 µsec)

The IEC61000-4-5 International Standard relates to the immunity requirements and test methods for electrical and electronic equipment subjected to Lighting conditions (surge 8 x 20 µsec).

Figure 9 shows an oscilloscope plot that illustrates and describes an 8 x 20 µsec pulse condition. This pulse is defined as double exponential since it is composed by two exponential factors, one of them defines the Rise time of the waveform (which in this case is 8.0 µsec) and the other one defines the decay time (which in this case is 20 µsec), this decay time is measured at 50% of the peak current value since it is the region in which the highest energy is dissipated.

According to the industrial standard IEC61000-4-5, this kind of waveform represents the waveform conditions generated due to lighting conditions.

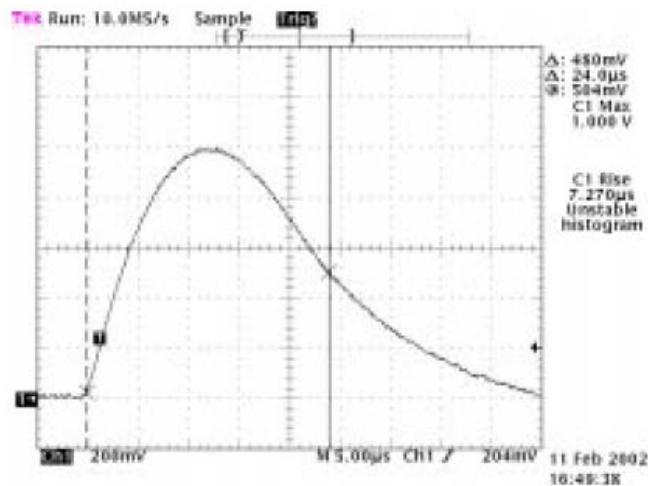


Figure 9 . Double Exponential Pulse 8 x 20 µsec

For these characterization purposes, a standard surge generator (8 x 20 µsec waveform) known as KeyTek tester model 424 was used. The surge test pulse is applied to the device between any of its I/O lines and ground, and the measurements to be taken are the peak current value (I_{pp}) and the clamping voltage (V_c) in the device.

Our UM5204EEXF device specify two different conditions for clamping voltage (V_p), these conditions are shown below:

- 15V Maximum @ $I_{pp} = 1.0$ A (8 x 20 µsec waveform)
- 25V Maximum @ $I_{pp} = 6.0$ A (8 x 20 µsec waveform)

Upon the previous device's characterizations and studies, it has been shown that the UM5204EEXF device from Union Semiconductor fully covers the main important features that any semiconductor products to be used in high data I/O lines applications for ESD protection must have.

Typical Applications Schemes for ESD Protection in High Speed I/O Lines

Video Interface Protection

Video interfaces are hot plugging/unplugging systems that are susceptible to receive electrostatic discharges (ESD) from users or air. These conditions can damage or even destroy the IC of the video interface if it is not protected. Because video interfaces are high speed data rate applications, it is necessary to use protection devices with extremely low capacitance and low leakage current so that the integrity of the video signal is not affected. In addition, protection devices must also offer the proper ESD ratings to cover the most common ESD industry standards (IEC 61000-4-2). The UM5204EEXF/UM5304EEXF device is designed to provide ESD protection in this type of applications. Figure 10 shows the typical applications scheme.

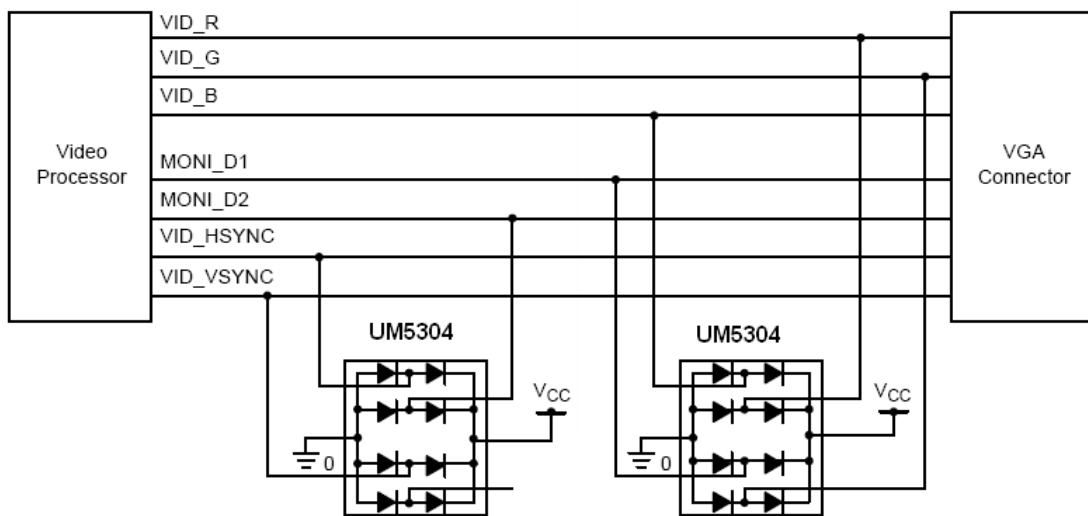


Figure 10

10 / 100 Ethernet Protection

Ethernet IC's are also susceptible to electrostatic discharges that can cause damage to them. Although the Ethernet chip may have some sort of integrated protection, it is unlikely that it can cover the ESD ratings specified by the international standard IEC 61000-4-2. Depending on the magnitude of the electrostatic discharge, it can cause hard or soft failures in the IC which will result in the malfunction of the system.

Ethernet is a local area network technology that transmits information between computers at speeds of 10 and 100Mbps. Currently the most widely used version of Ethernet technology is the 10Mbps twisted-pair variety. The 10Mbps Ethernet media varieties include the original thick coaxial system, as well as thin coaxial, twisted-pair, and fiber optic systems. The most recent Ethernet standard defines the new 100Mbps Fast Ethernet system which operates over twisted-pair and fiber optic media.

For the most typical Ethernet system, a twisted-pair consists of two differential signal pairs, one pair is for the transmitter and the other for the receiver. Electrostatic discharges can appear across the line pairs of the transmitter or receiver, which are induced to the Ethernet chip through the coupling of the transformer. Figure 11 shows a typical application scheme for protection in Ethernet applications, the protection is provided in differential mode.

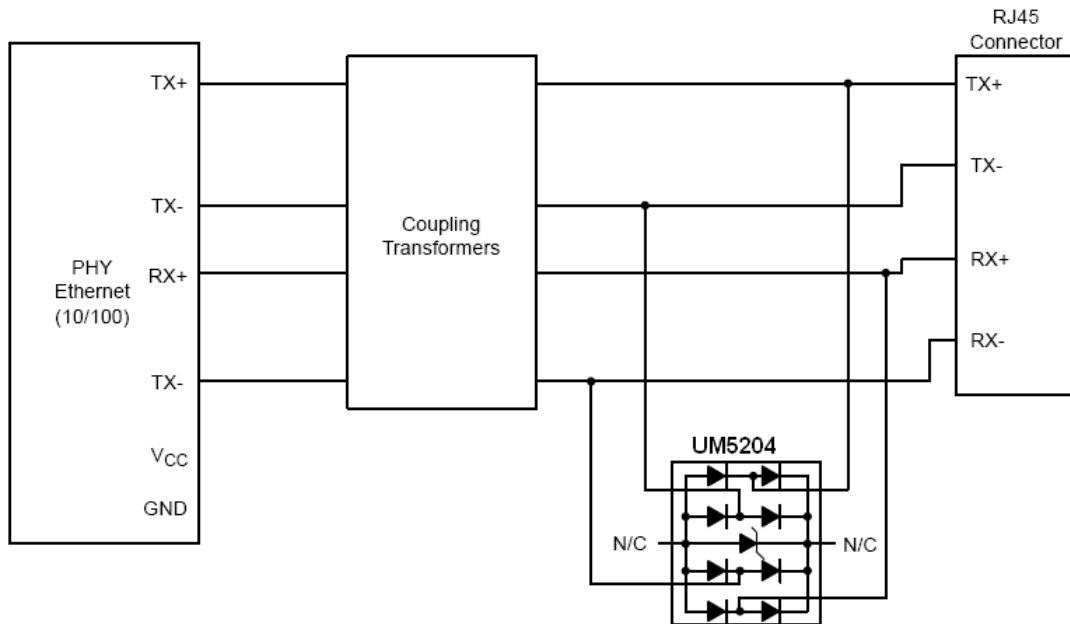


Figure 11. Protection for Ethernet 10/100 (Differential Mode)

Protection for USB Ports

ESD Protection in USB applications requires the usage of very sophisticated semiconductor devices capable to operate under conditions of high speed data transmission and the high technology of the USB controller, so conventional discrete methods to protect serial ports would be obsolete and non-efficient for USB applications. The UM5204EEXF devices provide unique integrated Low Capacitance TVS Diode Arrays designed to protect multiple four I/O lines, and also the power supply line against damage due to ESD conditions or transient voltage conditions. Figure 12 shows a typical applications scheme for USB protection.

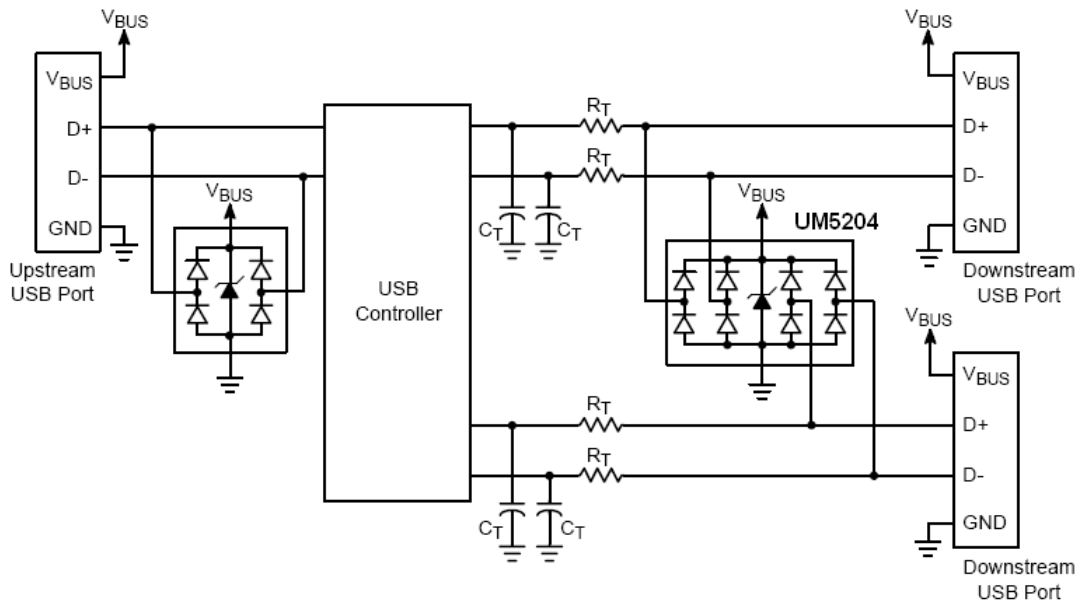


Figure12 . Protection for USB Ports

PCB Design Considerations

PCB design activities for USB applications is critical to meet the USB 2.0 and 1.1 requirements, so standard high frequency PCB design rules should be used in the layout to minimize any parasitic inductance and capacitance that may degrade the device's performance. It requires optimum component placement and good practices in circuit designing. Some general design guidelines are listed below to optimize the performance of the UM5204EEXF.

- Use ground planes to minimize the PCB's ground inductance.
- Critical signal lines should not be operated near board edges.
- D+ and D- signal line traces must not be operated near similar signal lines or high speed data transferring lines.
- Locate the UM5204EEXF device as close to the USB connector as possible to avoid transient coupling.
- Minimize the PCB trace lengths between the USB connector and the UM5204EEXF device.
- Minimize the PCB trace lengths for the ground return connections.

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