High–Speed CAN Transceiver with Standby Mode

UM3842S8S *SOP8*
UM3842S8 *SOP8*
UM3842DA *DFN8 3.0×3.0*

General Description

The UM3842 high–speed CAN transceiver provides an interface between a Controller Area Network (CAN) protocol controller and the physical two–wire CAN bus. The transceiver is designed for high–speed CAN applications in the automotive industry, providing the differential transmit and receive capability to (a microcontroller with) a CAN protocol controller. The UM3842 offers improved Electro Magnetic Compatibility (EMC) and Electro Static Discharge (ESD) performance, and also features:

- Ideal passive behavior to the CAN bus when the supply voltage is off
- A very low–current Standby mode with bus wake–up capability
- UM3842S8 and UM3842DA can be interfaced directly to microcontrollers with supply voltages from 3V to 5V

The UM3842 implements the CAN physical layer as defined in ISO 11898–2:2016 and SAE J2284–1 to SAE J2284–5. This implementation enables reliable communication in the CAN FD fast phase at data rates up to 5 Mbit/s. These features make the UM3842 an excellent choice for all types of HS–CAN networks, in nodes that require a low–power mode with wake–up capability via the CAN bus.

Applications

- High–speed CAN applications in the automotive industry
- Industrial
- Control

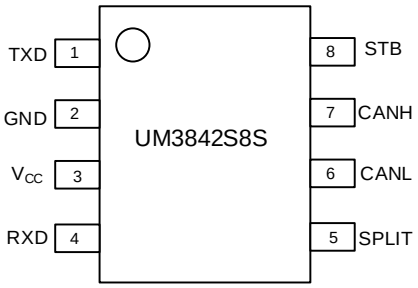
Features

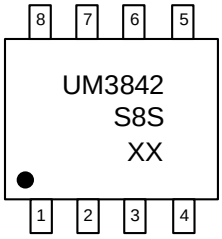
- ISO 11898–2:2016 and SAE J2284–1 to SAE J2284–5 compliant
- Timing guaranteed for data rates up to 5Mbit/s in the CAN FD fast phase
- V_{IO} input on UM3842S8 and UM3842DA allows for direct interfacing with 3 V to 5 V microcontrollers
- SPLIT voltage output on UM3842S8S for stabilizing the recessive bus level
- Available in SOP8 package and leadless DFN8 package (3.0 mm × 3.0 mm) with improved Automated Optical Inspection (AOI) capability
- AEC–Q100 compliant
- Very low-current Standby mode with host and bus wake-up capability
- Transmit Data (TXD) dominant time-out function
- Bus-dominant time-out function in Standby mode
- Undervoltage detection on pins V_{CC} and V_{IO}
- High ESD handling capability on the bus pins (±8 kV)
- High voltage robustness on CAN pins (±58V)
- Bus pins protected against transients in automotive environments

Ordering Information

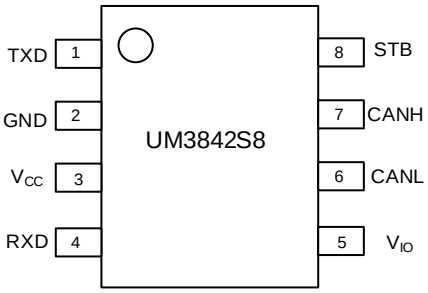
Part Number	Temp. Range	Marking	Package Type	Shipping Qty
UM3842S8S	－40°C to +125°C	UM3842S8S	SOP8	3000pcs/13Inch Tape & Reel
UM3842S8	－40°C to +125°C	UM3842S8	SOP8	3000pcs/13Inch Tape & Reel
UM3842DA	－40°C to +125°C	3842	DFN8 3.0×3.0	3000pcs/13Inch Tape & Reel

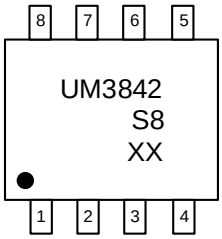
Pin Configuration　　Top View



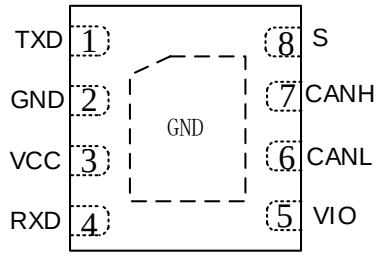


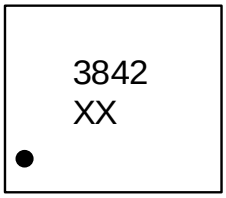
XX: Week Code
UM3842S8S
SOP8





XX: Week Code
UM3842S8
SOP8





XX: Week Code
UM3842DA
DFN8 3.0×3.0

Pin Description

Pin Number	Symbol	Function
1	TXD	Transmit data input
2	GND (Note1)	Ground supply
3	V_{CC}	Supply voltage
4	RXD	Receive data output; reads out data from the bus lines
5	SPLIT	Common–mode stabilization output; in UM3842S8S version only
5	V_{IO}	Supply voltage for I/O level adapter; in UM3842S8 and UM3842DA versions only
6	CANL	LOW–level CAN bus line
7	CANH	HIGH–level CAN bus line
8	STB	Standby mode control input

Note1: DFN8 package die supply ground is connected to both the GND pin and the exposed center pad. The GND pin must be soldered to board ground. For enhanced thermal and electrical performance, it is recommended that the exposed center pad also be soldered to board ground.

Absolute Maximum Ratings

In accordance with the Absolute Maximum Rating System (IEC 60134). All voltages are referenced to GND.

Parameter	Symbol	Conditions	Min	Max	Unit
Voltage on pin x (Note1)	V_X	On pins CANH, CANL and SPLIT	–58	+58	V
		On any other pin	–0.3	+7	V
Voltage between pin CANH and pin CANL	$V_{(CANH–CANL)}$		–27	+27	V
Transient voltage	V_{TRT}	On pins CANH, CANL (Note2)			
		Pulse 1	–100	–	V
		Pulse 2a	–	75	V
		Pulse 3a	–150	–	V
		Pulse 3b	–	100	V
Operating junction temperature	T_J	(Note3)	–40	+125	℃
Storage temperature	T_{STG}		–55	+150	℃

Note1: The device can sustain voltages up to the specified values over the product lifetime, provided applied voltages (including transients) never exceed these values.

Note2: According to IEC TS 62228 (2007), Section 4.2.4; parameters for standard pulses defined in ISO7637 part 2: 2004–06.

Note3: In accordance with IEC 60747–1. An alternative definition of operating junction temperature is: $T_j=T_A+P\times\theta_{JA}$, where θ_{JA} is a fixed value to be used for the calculation of T_j. The rating for T_J limits the allowable combinations of power dissipation (P) and ambient temperature (T_A).

Thermal Characteristic (Note1)

Symbol	Parameter	UM3842 S8	UM3843 S8	UM3842 DA	Unit
θ_{JA}	Junction-to-ambient thermal resistance	110	110	55	°C/W

Note1: According to IEC 60747–1.

Electrical Characteristics (Static)

T_J = –40 °C to +125 °C; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1); R_L = 60Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC (Note2).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply; pin V_{CC}						
Supply Voltage	V_{CC}		4.5	–	5.5	V
Undervoltage detection voltage on pin V_{CC}	$V_{uvd(VCC)}$		3.5	–	4.5	V
Supply Current	I_{CC}	Standby mode				
		UM3842S8S; includes I_{IO}; V_{TXD} = V_{IO} (Note3)	–	10	15	μA
		UM3842S8 or UM3842DA	–	–	5	μA
		Normal mode				
		Recessive; V_{TXD} =V_{IO} (Note3))	2.5	5	10	mA
		Dominant; V_{TXD} = 0 V	20	45	70	mA
		Dominant; V_{TXD}=0 V; short circuit on bus lines; –3 V<(V_{CANH}=V_{CANL})<+18V	2.5	80	110	mA
I/O level adaptor supply; pin V_{IO} (Note1)						
Supply voltage on pin V_{IO}	V_{IO}		2.8	–	5.5	V
Undervoltage detection voltage on pin V_{IO}	$V_{uvd(VIO)}$		1.3	2.0	2.7	V
Supply current on pin V_{IO}	I_{IO}	Standby mode; V_{TXD}=V_{IO} (Note3)	5	–	13	μA
		Normal mode				
		Recessive; V_{TXD} = V_{IO} (Note3)	14	80	200	μA
		Dominant; V_{TXD} = 0 V	–	350	1000	μA

Electrical Characteristics (Static)——continued

T_J = –40 ℃ to +125 ℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1); R_L = 60Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC (Note2).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Standby mode control input; pin STB						
HIGH–level input voltage	V_{IH}	(Note4)	$0.7V_{IO}$ (Note3)	–	V_{IO}+ 0.3 (Note3)	V
LOW–level input voltage	V_{IL}		–0.3	–	$0.3V_{IO}$ (Note3)	V
HIGH–level input current	I_{IH}	$V_{STB} = V_{IO}$ (Note3)	1	–	+1	μA
LOW–level input current	I_{IL}	V_{STB} = 0 V	–15	–	–1	μA
CAN transmit data input; pin TXD						
HIGH–level input voltage	V_{IH}	(Note4)	$0.7V_{IO}$ (Note3)	–	V_{IO}+0.3 (Note3)	V
LOW–level input voltage	V_{IL}		0.3	–	$+0.3V_{IO}$ (Note3)	V
HIGH–level input current	I_{IH}	$V_{TXD} = V_{IO}$ (Note3)	–5	–	+5	μA
LOW–level input current	I_{IL}	V_{TXD} = 0 V	–260	–150	–30	μA
Input capacitance	Ci	(Note5)	–	5	10	pF
CAN receive data output; pin RXD						
HIGH–level output current	I_{OH}	$V_{RXD} = V_{IO}$ – 0.4V (Note3)	–8	–3	–1	mA
LOW–level output current	I_{OL}	V_{RXD} = 0.4V; bus dominant	2	5	12	mA
Bus lines; pins CANH and CANL						
Dominant output voltage	$V_{O(dom)}$	V_{TXD} = 0 V; $t < t_{to(dom)TXD}$				
		pin CANH; R_L = 50Ω to 65Ω	2.75	3.5	4.5	V
		pin CANL; R_L = 50Ω to 65Ω	0.5	1.5	2.25	V
Transmitter dominant voltage symmetry	$V_{dom(TX)sym}$	$V_{dom(TX)sym} = V_{CC}–V_{CANH} – V_{CANL}$	–400	–	+400	mV
Transmitter voltage symmetry	V_{TXsym}	$V_{TXsym}= V_{CANH} + V_{CANL}$ (Note5); f_{TXD} = 250 kHz, 1MHz and 2.5MHz (Note6); V_{CC} = 4.75V to 5.25 V; C_{SPLIT} = 4.7 nF	$0.9V_{CC}$	–	$1.1V_{CC}$	V

Electrical Characteristics (Static)——continued

T_J = –40 °C to +125°C; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1); R_L = 60Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC (Note2).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Differential output voltage	$V_{O(dif)}$	Dominant: Normal mode; V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 4.75 V to 5.25 V				
		R_L = 45Ω to 65Ω	1.5	–	3	V
		R_L = 45Ω to 70Ω	1.5	–	3.3	V
		R_L = 2240Ω	1.5	–	5	V
		recessive; no load				
		Normal mode: V_{TXD} = V_{IO} (Note3)	–50	–	+50	mV
		Standby mode	–0.2	–	+0.2	V
Recessive output voltage	$V_{O(rec)}$	Normal mode; V_{TXD} = V_{IO} (Note3) no load	2	$0.5V_{CC}$	3	V
		Standby mode； no load	–0.1	–	+0.1	V
Differential receiver threshold voltage	$V_{th(RX)dif}$	–30 V≤V_{CANL} ≤+30 V; –30 V≤V_{CANH} ≤+30 V				
		Normal mode;	0.5	0.7	0.9	V
		Standby mode (Note7)	0.4	0.7	1.15	
Receiver recessive voltage	$V_{rec(RX)}$	–30 V≤V_{CANL} ≤+30 V; –30 V≤V_{CANH} ≤+30 V				
		Normal mode;	–4	–	0.5	V
		Standby mode	–4	–	0.4V	V
Receiver dominant voltage	$V_{dom(RX)}$	–30 V≤V_{CANL} ≤+30 V; –30 V≤V_{CANH} ≤+30 V				
		Normal mode;	0.9	–	9.0	V
		Standby mode	1.15	–	9.0	V
Differential receiver hysteresis voltage	$V_{hys(RX)dif}$	–30 V≤V_{CANL} ≤+30 V; –30 V≤V_{CANH} ≤+30 V	50	120	200	mV
Dominant short–circuit output current	$I_{O(sc)dom}$	V_{TXD} = 0 V; t < $t_{to(dom)TXD}$; V_{CC} = 5 V				
		pin CANH; V_{CANH} = –15V to+40V	–100	–70	–40	mA
		pin CANL; V_{CANL} = –15V to +40 V	40	70	100	mA

Electrical Characteristics (Static)——continued

T_J = –40 ℃ to +125 ℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1); R_L = 60Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC (Note2).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Recessive short–circuit output current	$I_{O(sc)rec}$	Norma mode; V_{TXD} = V_{IO} (Note3); V_{CANH}= V_{CANL}= –27V to +32 V	–5	–	+5	mA
Leakage current	I_L	V_{CC} = V_{IO} = 0 V or V_{CC} = V_{IO} = shorted to ground via 47 kΩ; V_{CANH} = V_{CANL} = 5 V	–5	-	+5	μA
Input resistance	R_i	–2 V≤ V_{CANL} ≤+7 V; (Note5) –2 V≤ V_{CANH} ≤+7 V	9	15	28	kΩ
Input resistance deviation	ΔR_i	0 V≤ V_{CANL}≤ +5 V; (Note5) 0 V≤ V_{CANH}≤ +5 V	–1	–	+1	%
Differential input resistance	$R_{i(dif)}$	–2 V≤ V_{CANL}≤ +7 V; (Note5) –2 V≤ V_{CANH}≤ +7 V	19	30	52	kΩ
Common–mode input capacitance	$C_{i(cm)}$	(Note5)	–	–	20	pF
Differential input capacitance	$C_{i(dif)}$	(Note5)	–	–	10	pF
Common mode stabilization output; pin SPLIT; only for UM3842S8S						
V_O	Output voltage	Normal mode; I_{SPLIT}= –500μA to +500μA	0.3V_{CC}	0.5V_{CC}	0.7V_{CC}	V
		Normal mode; R_L=1MΩ	0.45V_{CC}	0.5V_{CC}	0.55V_{CC}	V
I_L	Leakage current	Standby mode V_{SPLIT} = -58V to +58V	–5	–	+5	μA

Electrical Characteristics (Static)——continued

T_J = –40 ℃ to +125 ℃; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1); R_L = 60Ω unless specified otherwise; All voltages are defined with respect to ground; Positive currents flow into the IC (Note2).

ESD Ratings				
Parameter	**Symbol**		**Value**	**Unit**
		IEC 61000–4–2 (150 pF, 330Ω) (Note8)		
		At pins CANH and CANL	±8000	kV
		Human Body Model (HBM); 100 pF, 1.5 kΩ (Note9)		
		At pins CANH and CANL	±8000	kV
		At any other pin	±4000	kV
		Machine Model (MM); 200 pF, 0.75 μH, 10Ω (Note10)		
		At any pin	±300	
		Charged Device Model (CDM); field Induced charge; 4 pF (Note11)		
		At corner pins	±750	V
		At any pin	±500	V

Note1： Only UM3842S8 and UM3842DA have a V_{IO} pin. With UM3842S8S, the V_{IO} input is internally connected to V_{CC}.

Note2： All parameters are guaranteed over the operating junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and power supply voltage range.

Note3： V_{IO} = V_{CC} for the non–V_{IO} product variants UM3842S8S

Note4： Maximum value assumes V_{CC} < V_{IO}; if V_{CC} > V_{IO}, the maximum value will be V_{CC} + 0.3V.

Note5: Not tested in production; guaranteed by design.

Note6： The test circuit used to measure the bus output voltage symmetry (which includes C_{SPLIT}) is shown in Figure 9.

Note7： For UM3842S8 and UM3842DA: values valid when V_{IO} = 4.5V to 5.5V; when V_{IO} = 2.8V to 4.5V, values valid when –12 V ≤ V_{CANL} ≤ +12 V, –12 V ≤ V_{CANH} ≤ +12 V.

Note8: According to IEC TS 62228 (2007), Section 4.3; DIN EN 61000–4–2.

Note9: According to AEC–Q100–002.

Note10: According to AEC–Q100–003.

Note11: AEC–Q100–011 Rev–C1. The classification level is C4B.

Electrical Characteristics (Dynamic)

T_J = –40 °C to +125 °C; V_{CC} = 4.5V to 5.5V; V_{IO} = 2.8V to 5.5V (Note1)； R_L = 60Ω unless specified otherwise. All voltages are defined with respect to ground. Positive currents flow into the IC (Note2).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Transceiver timing; pins CANH, CANL, TXD and RXD； see Figure 1 and Figure 8						
Delay time from TXD to bus dominant	$t_{d(TXD–busdom)}$	Normal mode	–	65	–	ns
Delay time from TXD to bus recessive	$t_{d(TXD–bussrec)}$	Normal mode	–	90	–	ns
Delay time from bus dominant to RXD	$t_{d(busdom–RXD)}$	Normal mode	–	60	–	ns
Delay time from bus recessive to RXD	$t_{d(busrec–RXD)}$	Normal mode	–	65	–	ns
Delay time from TXD LOW to RXD LOW	$t_{d(TXDL–RXDL)}$	Version with SPLIT pin; Normal mode	60	–	220	ns
		Versions with V_{IO} pin; Normal mode	60	–	250	ns
Delay time from TXD HIGH to RXD HIGH	$t_{d(TXDH–RXDH)}$	Version with SPLIT pin; Normal mode	60	–	220	ns
		Versions with V_{IO} pin; Normal mode	60	–	250	ns
Transmitted recessive bit width	$t_{bit(bus)}$	$t_{bit(TXD)}$ = 500 ns（Note3）	435	–	530	ns
		$t_{bit(TXD)}$ = 200 ns（Note3）	155	–	210	ns
Bit time on pin RXD	$t_{bit(RXD)}$	$t_{bit(TXD)}$ = 500 ns（Note3）	400	–	550	ns
		$t_{bit(TXD)}$ = 200 ns（Note3）	120	–	220	ns
Receiver timing symmetry	Δt_{rec}	$t_{bit(TXD)}$ = 500 ns	–65	–	+40	ns
		$t_{bit(TXD)}$ = 200 ns	–45	–	+15	ns
TXD dominant time–out time	$t_{to(dom)TXD}$	V_{TXD} = 0 V; Normal mode（Note4）	0.3	2	5	ms
Bus dominant time-out time	$t_{to(dom)bus}$	Standby mode	0.3	2	5	ms
Bus wake-up filter time	$t_{fltr(wake)bus}$	Version with SPLIT pin Standby mode	0.5	1	3	µs
		Versions with V_{IO} pin Standby mode	0.5	1.5	5	µs
Standby to normal mode delay time	$t_{d(stb-norm)}$		7	25	47	µs

Note1： Only UM3842S8 and UM3842DA have a V_{IO} pin. In transceivers without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}.

Note2： All parameters are guaranteed over the operating junction temperature range by design. Factory testing uses correlated test conditions to cover the specified temperature and

power supply voltage range.

Note3： See Figure 2.

Note4： Minimum value of 0.8ms required according to SAE J2284; 0.3ms is allowed according to ISO11898–2:2016 for legacy devices.

Parameter Measurement Information

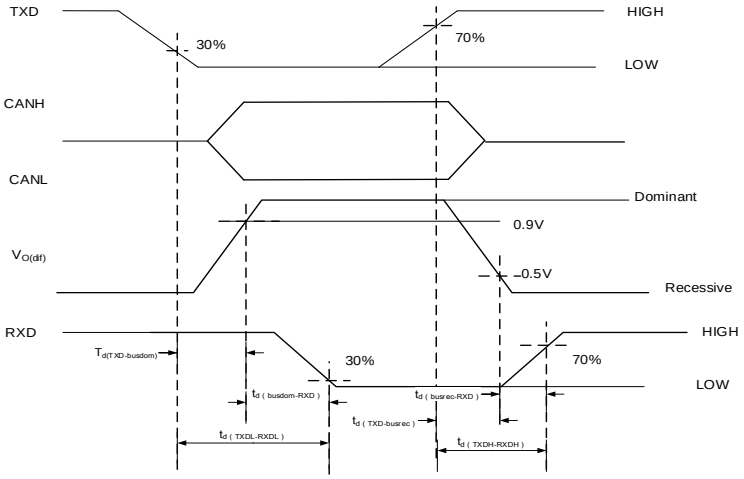


Figure 1. CAN transceiver timing diagram

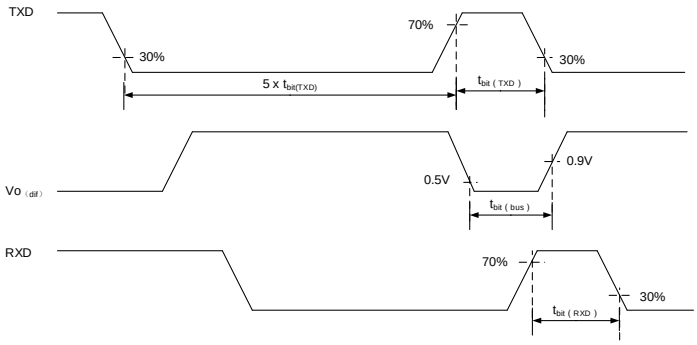


Figure 2. CAN FD timing definitions according to ISO 11898–2:2015

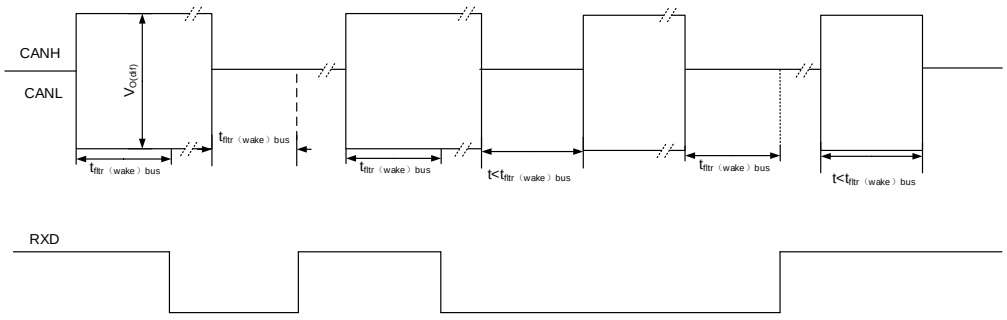
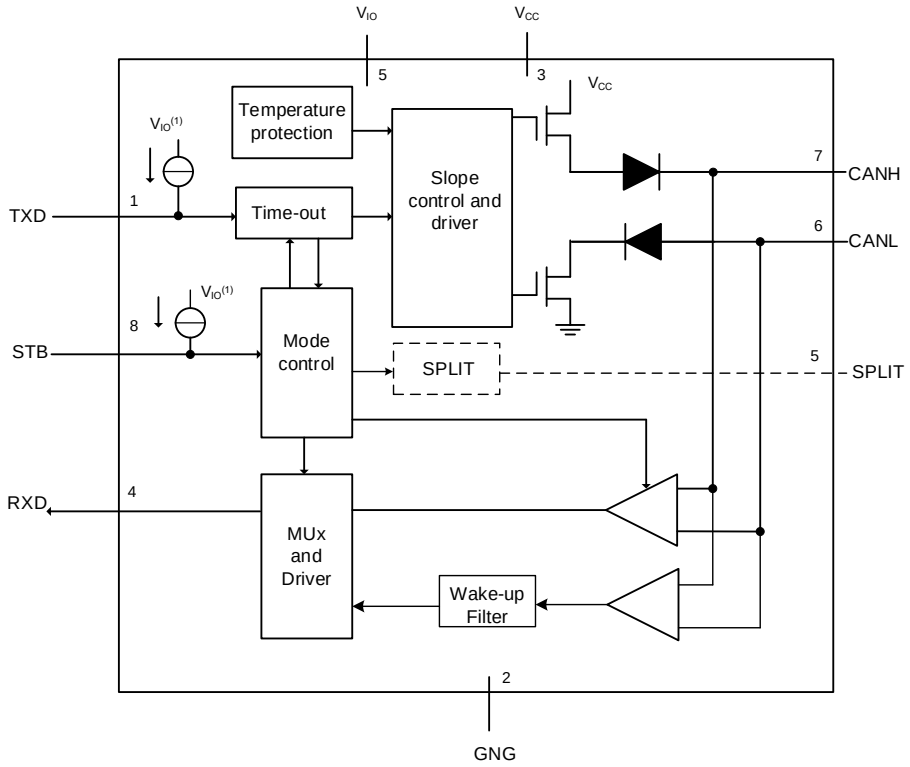


Figure 3. Wake-up timing

Detailed Functional Block Diagram



(1) In a transceiver with a SPLIT pin, the V_{IO} input is internally connected to V_{CC}.

Figure 4. Block diagram

Functional Description

The UM3842 is a HS-CAN stand-alone transceiver with Standby mode. They improve EMC and ESD handling capability and quiescent current performance. Improved slope control and high DC handling capability on the bus pins provide additional application flexibility. The UM3842 is available in two versions, distinguished only by the function of pin 5:

- The UM3842 is backwards compatible with the TJA1040 when used with a 5 V microcontroller, and also covers existing PCA82C250 and PCA82C251 applications
- The UM3842S8 and UM3842DA allow for direct interfacing to microcontrollers with supply voltages down to 3 V

Operating modes

The UM3842 supports two operating modes, Normal and Standby, which are selected via pin STB. The description of the operating modes under normal supply conditions is shown below.

Operating modes

Mode	Pin STB	Pin RXD	
		Low	High
Normal	Low	Bus dominant	Bus recessive
Standby	High	Wake-up request detected	No wake-up request detected

Normal mode: A LOW level on pin STB selects Normal mode. In this mode, the transceiver can transmit and receive data via the bus lines CANH and CANL (see Figure 4 for the block diagram). The differential receiver converts the analog data on the bus lines into digital data which is output to pin RXD. The slopes of the output signals on the bus lines are controlled internally and are

optimized in a way that guarantees the lowest possible EME.

Standby mode: A HIGH level on pin STB selects Standby mode. In Standby mode, the transceiver is not able to transmit or correctly receive data via the bus lines. The transmitter and Normal-mode receiver blocks are switched off to reduce supply current, and only a low-power differential receiver monitors the bus lines for activity. The wake-up filter on the output of the low-power receiver does not latch bus dominant states, but ensures that only bus dominant and bus recessive states that persist longer than $t_{fltr(wake)bus}$ are reflected on pin RXD.
In Standby mode, the bus lines are biased to ground to minimize the system supply current. The low-power receiver is supplied by V_{IO}, and is capable of detecting CAN bus activity even if V_{IO} is the only supply voltage available. When pin RXD goes LOW to signal a wake-up request, a transition to Normal mode will not be triggered until STB is forced LOW.

Fail–Safe Features

TXD dominant time–out function: A 'TXD dominant time–out' timer is started when pin TXD is set LOW. If the LOW state on pin TXD persists for longer than $t_{to(dom)TXD}$, the transmitter is disabled, releasing the bus lines to recessive state. This function prevents a hardware and/or software application failure from driving the bus lines to a permanent dominant state (blocking all network communications). The TXD dominant time–out timer is reset when pin TXD is set to HIGH. The TXD dominant time–out time also defines the minimum possible bit rate of 40 kbit/s.

Bus dominant time-out function: In Standby mode a 'bus dominant time-out' timer is started when the CAN bus changes from recessive to dominant state. If the dominant state on the bus persists for longer than $t_{to(dom)bus}$, the RXD pin is reset to HIGH. This function prevents a clamped dominant bus (due to a bus short-circuit or a failure in one of the other nodes on the network) from generating a permanent wake-up request. The bus dominant time-out timer is reset when the CAN bus changes from dominant to recessive state.

Internal biasing of TXD and STB input pins: Pins TXD and STB have internal pull-ups to V_{IO} to ensure a safe, defined state in case one or both of these pins are left floating. Pull-up currents flow in these pins in all states; both pins should be held HIGH in Standby mode to minimize standby current.

Undervoltage detection on pins V_{CC} and V_{IO}: Should V_{CC} drop below the V_{CC} undervoltage detection level, $V_{uvd(VCC)}$, the transceiver will switch to Standby mode. The logic state of pin STB will be ignored until V_{CC} has recovered. Should V_{IO} drop below the V_{IO} undervoltage detection level, $V_{uvd(VIO)}$, the transceiver will switch off and disengage from the bus (zero load) until V_{IO} has recovered.

Overtemperature protection: The output drivers are protected against overtemperature conditions. If the operating junction temperature exceeds the shutdown junction temperature, $T_{j(sd)}$, the output drivers will be disabled until the operating junction temperature falls below $T_{j(sd)}$ and TXD becomes recessive again. Including the TXD condition ensures that output driver oscillations due to temperature drift are avoided.

SPLIT output pin and V_{IO} supply pin

Two versions of the UM3842 are available, only differing in the function of a single pin. Pin 5 is either a SPLIT output pin or a V_{IO} supply pin.

SPLIT pin: Using the SPLIT pin on the UM3842S8S in conjunction with a split termination network (see Figure 5 and Figure 6) can help to stabilize the recessive voltage level on the bus. This

will reduce EME in networks with DC leakage to ground (e.g., from deactivated nodes with poor bus leakage performance). In Normal mode, pin SPLIT delivers a DC output voltage of $0.5V_{CC}$. In Standby mode or when V_{CC} is off, pin SPLIT is floating. When not used, the SPLIT pin should be left open.

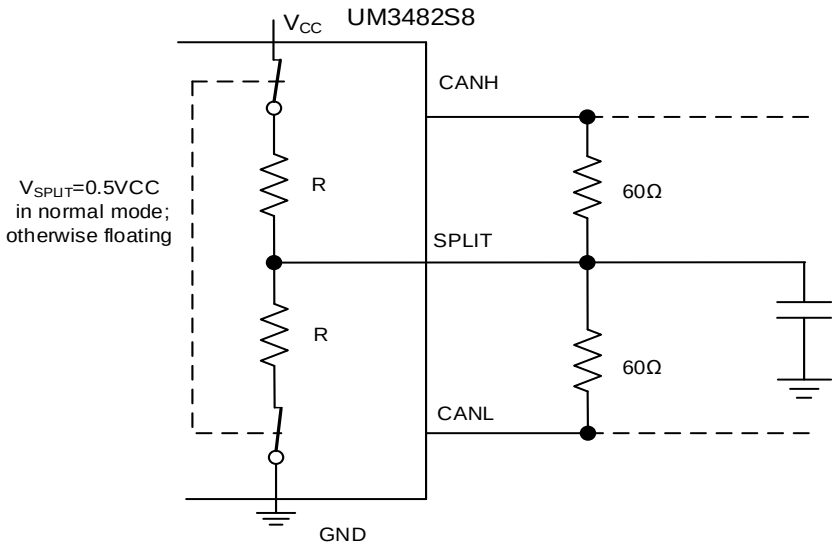
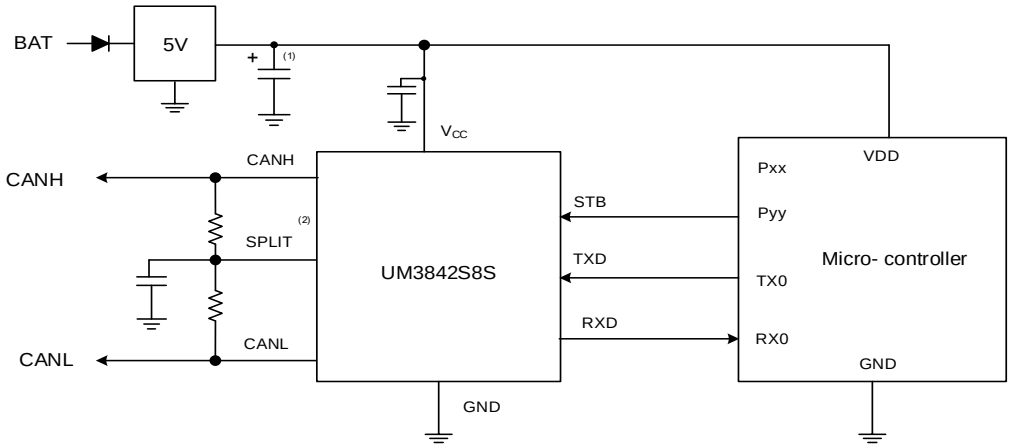


Figure 5. Stabilization circuitry and application for version with SPLIT pin

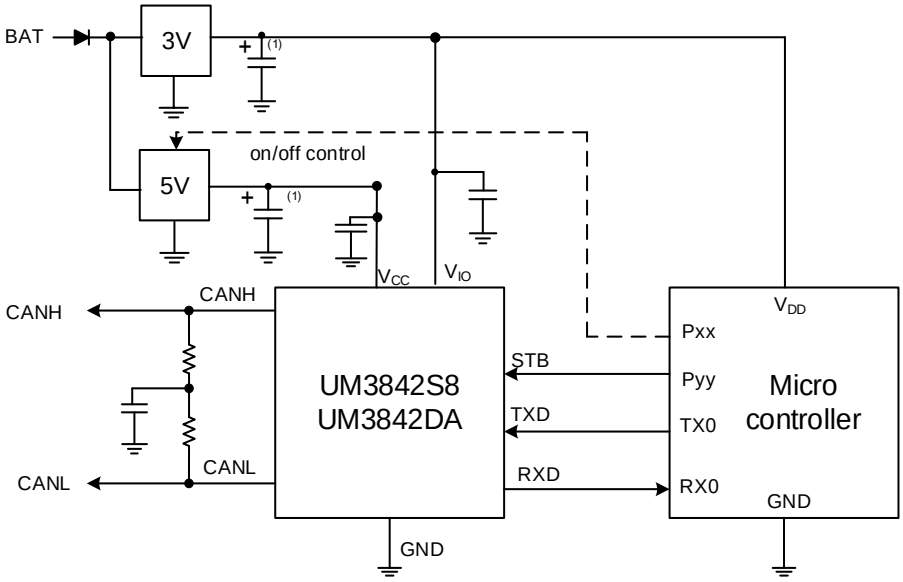
V_{IO} supply pin: Pin V_{IO} on the UM3842S8 and UM3842DA should be connected to the microcontroller supply voltage (see Figure 7). This will adjust the signal levels of pins TXD, RXD and STB to the I/O levels of the microcontroller. Pin V_{IO} also provides the internal supply voltage for the low-power differential receiver of the transceiver. For applications running in low-power mode, this allows the bus lines to be monitored for activity even if there is no supply voltage on pin V_{CC}. For versions of the UM3842without a V_{IO} pin, the V_{IO} input is internally connected to V_{CC}. This sets the signal levels of pins TXD, RXD and STB to levels compatible with 5 V microcontrollers.

Application Information



(1) Optional, depends on regulator.
(2) Optional common mode stabilization by a voltage source of $V_{CC}/2$ at pin SPLIT.

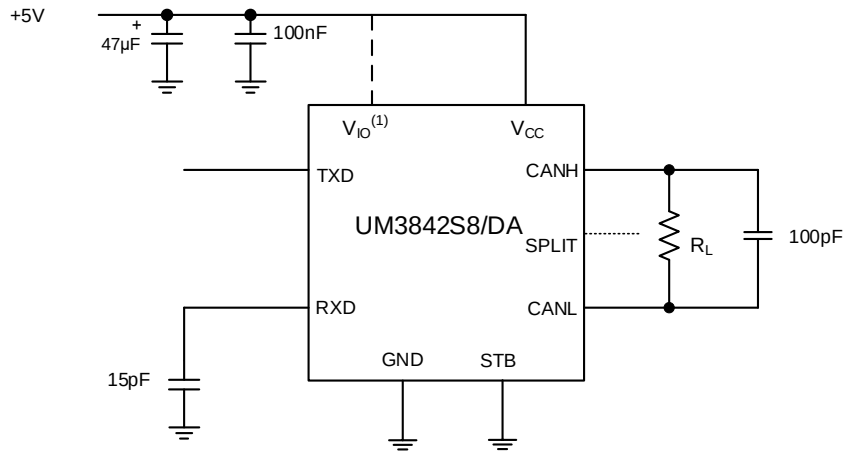
Figure 6. Typical application of the UM3842S8S



(1) Optional, depends on regulator.

Figure 7. Typical application with UM3842S8 or UM3842DA and a 3V microcontroller

Test Information



(1) For versions with a V_{IO} pin (UM3842S8 or UM3842DA) the V_{IO} pin is connected to pin V_{CC}.

Figure 8. Timing test circuit for CAN transceiver

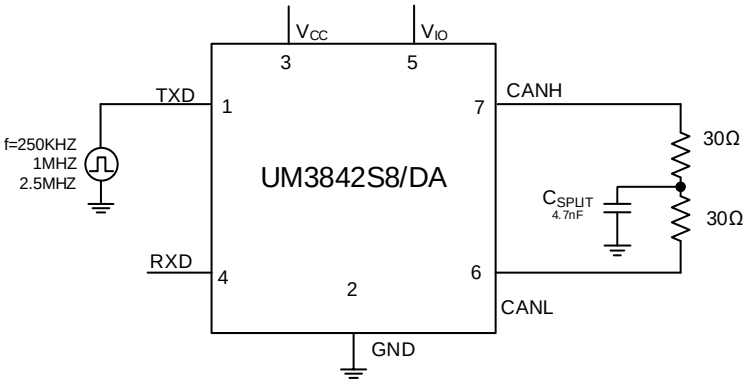
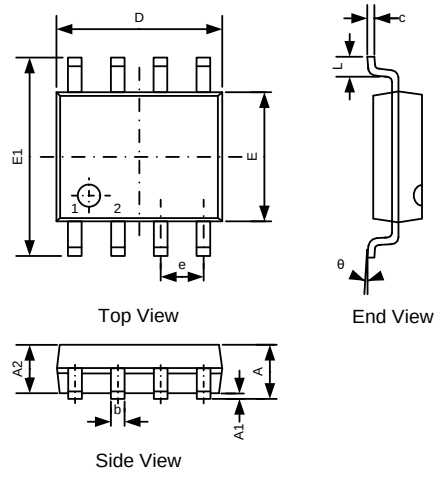


Figure 9. Test circuit for measuring transceiver driver symmetry

Package Information

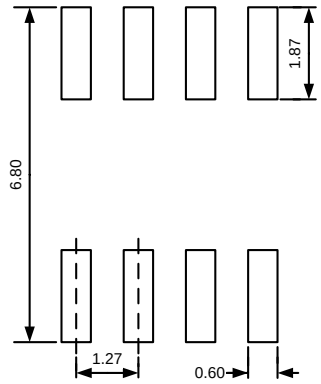
UM3842S8S SOP8

Outline Drawing



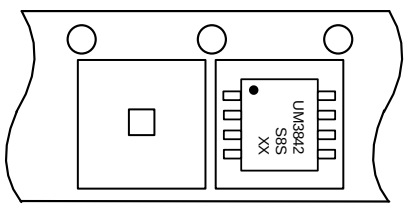
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	–	0.25	0.004	–	0.010
A2	1.25	–	1.65	0.049	–	0.065
b	0.30	–	0.51	0.012	–	0.020
c	0.15	–	0.25	0.006	–	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.80	3.90	4.00	0.150	0.154	0.157
E1	5.80	6.00	6.20	0.228	0.236	0.244
e	1.27BSC			0.050 BSC		
L	0.40	–	1.27	0.015	–	0.050
θ	0°	–	8°	0°	–	8°

Land Pattern



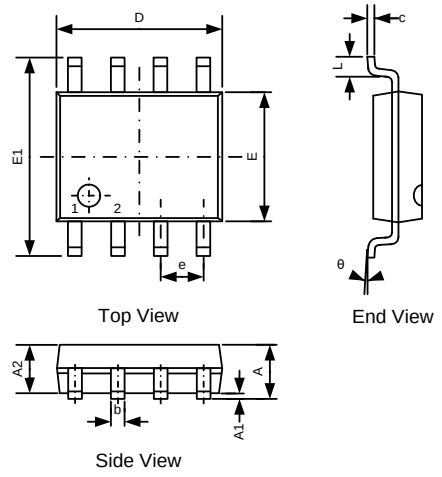
NOTES:
1. Compound dimension: 4.90×3.90;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



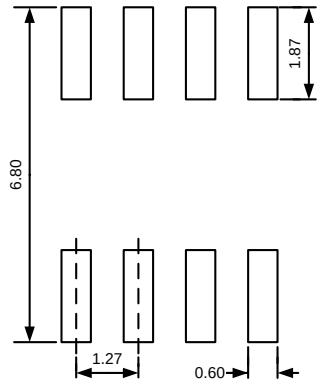
UM3842S8 SOP8

Outline Drawing



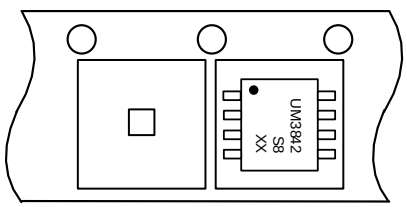
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	1.35	1.55	1.75	0.053	0.061	0.069
A1	0.10	–	0.25	0.004	–	0.010
A2	1.25	–	1.65	0.049	–	0.065
b	0.30	–	0.51	0.012	–	0.020
c	0.15	–	0.25	0.006	–	0.010
D	4.70	4.90	5.10	0.185	0.193	0.200
E	3.80	3.90	4.00	0.150	0.154	0.157
E1	5.80	6.00	6.20	0.228	0.236	0.244
e	1.27BSC			0.050 BSC		
L	0.40	–	1.27	0.015	–	0.050
θ	0°	–	8°	0°	–	8°

Land Pattern



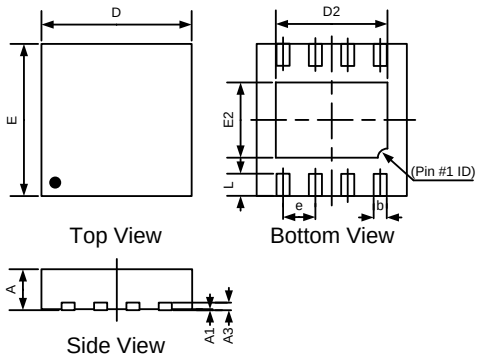
NOTES:
1. Compound dimension: 4.90×3.90;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



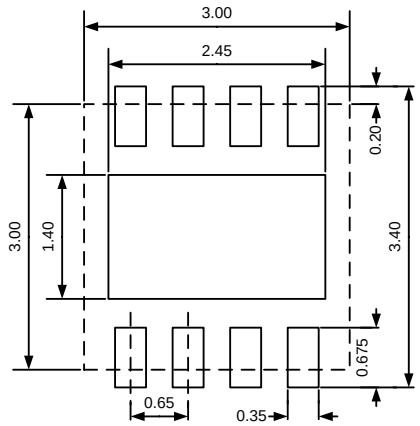
UM3842DA DFN8 3.0×3.0

Outline Drawing



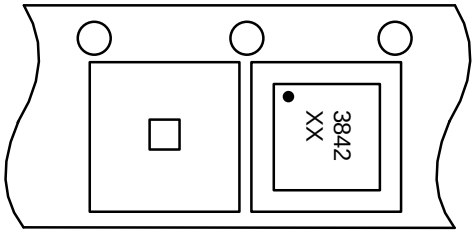
Symbol	DIMENSIONS					
	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.57	–	0.80	0.022	–	0.031
A1	0.00	–	0.05	0.000	–	0.002
A3	0.20REF			0.008REF		
b	0.20	–	0.35	0.008	–	0.014
D	2.924	3.00	3.076	0.115	0.118	0.121
D2	2.15	–	2.55	0.085	–	0.100
E	2.924	3.00	3.076	0.115	0.118	0.121
E2	1.40	–	1.75	0.055	–	0.069
e	0.65BSC			0.026BSC		
L	0.30	–	0.60	0.012	–	0.024

Land Pattern



NOTES:
1. Compound dimension: 3.00×3.00;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



GREEN COMPLIANCE

Union Semiconductor is committed to environmental excellence in all aspects of its operations including meeting or exceeding regulatory requirements with respect to the use of hazardous substances. Numerous successful programs have been implemented to reduce the use of hazardous substances and/or emissions.
All Union components are compliant with the RoHS directive, which helps to support customers in their compliance with environmental directives. For more green compliance information, please visit:
http://www.union–ic.com/index.aspx?cat_code=RoHSDeclaration

IMPORTANT NOTICE

The information in this document has been carefully reviewed and is believed to be accurate. Nonetheless, this document is subject to change without notice. Union assumes no responsibility for any inaccuracies that may be contained in this document, and makes no commitment to update or to keep current the contained information, or to notify a person or organization of any update. Union reserves the right to make changes, at any time, in order to improve reliability, function or design and to attempt to supply the best product possible.

Union Semiconductor, Inc
Add: Unit 606, No.570 Shengxia Road, Shanghai 201210
Tel: 021–51093966
Fax: 021–51026018
Website: www.union–ic.com