4-Bit Bidirectional Voltage-Level Translator for Open-Drain and Push-Pull Application

UM3284Q *QFN14 3.5×3.5*
UM3284QT *QFN12 1.7×2.0*
UM3284UE *TSSOP14*

General Description

The UM3284 is 4-channel ESD-protected level translator provides the level shifting necessary to allow data transfer in a multi-voltage system. Externally applied voltages, V_{CCB} and V_{CCA}, set the logic levels on either side of the device. A low-voltage logic signal present on the V_{CCA} side of the device appears as a high-voltage logic signal on the V_{CCB} side of the device, and vice-versa. The UM3284 bidirectional level translator utilizes a transmission-gate based design to allow data translation in either direction (V_{CCA}↔V_{CCB}) on any single data line. The UM3284 accepts V_{CCA} from +1.2V to +3.6V and V_{CCB} from +1.65V to +5.5V, making it ideal for data transfer between low-voltage ASICs / PLDs and higher voltage systems.

The UM3284 enters a three-state output mode to reduce supply current when output enable (OE) is low. The UM3284 is designed so that the OE input circuit is supplied by V_{CCA}. ±8kV ESD protection on the V_{CCB} side for greater protection in applications that route signals externally.

The UM3284Q is available in QFN14 3.5×3.5 package. The UM3284QT is available in QFN12 1.7×2.0 package and the UM3284UE is available in TSSOP14 package.

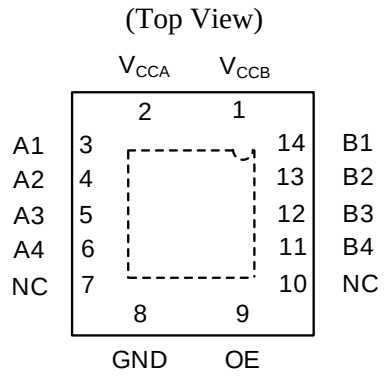
Applications

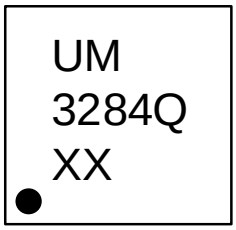
- Handsets
- Smart phones
- Tablets
- Desktop PCs

Features

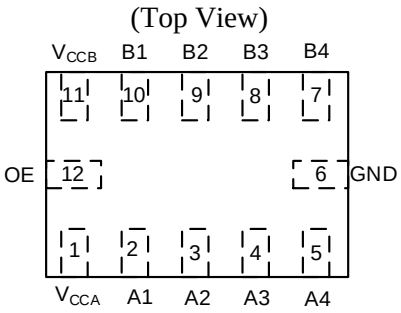
- Max Data Rates:
  110Mbps(Push Pull),
  1.2Mbps(Open Drain)
- 1.2V to 3.6V on A port and 1.65V to 5.5V on B port(V_{CCA}≤V_{CCB})
- No Direction-Control Signal Needed
- No Power-Supply Sequencing Required V_{CCA} or V_{CCB} Can Be Ramped First
- Low Power Consumption
- ±8kV ESD Protection on B port
- Latch-Up Performance Exceeds 100mA

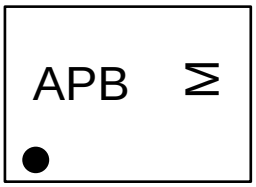
Pin Configurations **Top View**



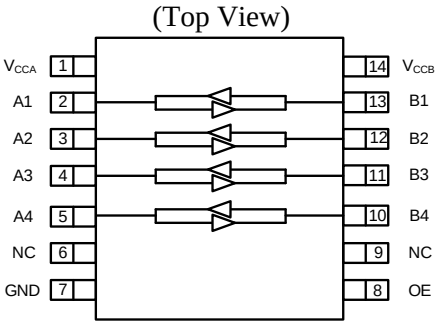


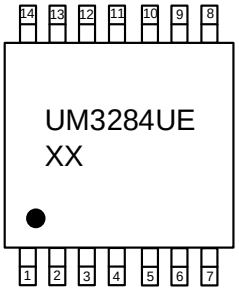
XX: Week Code
UM3284Q
QFN14 3.5×3.5





M: Month Code
UM3284QT
QFN12 1.7×2.0





XX: Week Code
UM3284UE
TSSOP14

Pin Description

Pin Name	Function
A1	Input/Output 1. Referenced to V_{CCA}
V_{CCA}	A-Port supply voltage. $1.2V \le V_{CCA} \le 3.6V$ and $V_{CCA} \le V_{CCB}$
A2	Input/Output 2. Referenced to V_{CCA}
A3	Input/Output 3. Referenced to V_{CCA}
A4	Input/Output 4. Referenced to V_{CCA}
OE	3-state output enable. Pull OE low to place all outputs in 3-state mode. Referenced to V_{CCA}
GND	Ground
B4	Input/Output 4. Referenced to V_{CCB}
B3	Input/Output 3. Referenced to V_{CCB}
B2	Input/Output 2. Referenced to V_{CCB}
V_{CCB}	B-Port supply voltage. $1.65V \le V_{CCB} \le 5.5V$
B1	Input/Output 1. Referenced to V_{CCB}

Ordering Information

Part Number	Packaging Type	Marking Code	Shipping Qty
UM3284Q	QFN14 3.5×3.5	UM3284Q	3000pcs/13Inch Tape & Reel
UM3284QT	QFN12 1.7×2.0	APB	3000pcs/7Inch Tape & Reel
UM3284UE	TSSOP14	UM3284UE	3000pcs/13Inch Tape & Reel

Absolute Maximum Ratings (Note 1)

Over operating free-air temperature range (unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{CCA}	Supply Voltage Range		-0.5 to +4.5	V
V_{CCB}	Supply Voltage Range		-0.5 to +6.5	V
V_I	Input Voltage Range	A ports	-0.5 to +4.5	V
		B ports	-0.5 to +6.5	
V_O	Voltage Range applied to any output in the high-impedance or power-off state	A ports	-0.5 to +4.5	V
		B ports	-0.5 to +6.5	
V_O	Voltage Range applied to any output in the high or low state (Note 2)	A ports	-0.5 to (V_{CCA}+0.5)	V
		B ports	-0.5 to (V_{CCB}+0.5)	
I_{IK}	Input Clamp Current	V_I＜0	-50	mA
I_{OK}	Output Clamp Current	V_O＜0	-50	mA
I_O	Continuous Output Current		±50	mA
	Continuous Current through V_{CCA}, V_{CCB}, or GND		±100	mA
T_{OP}	Operating Temperature Range		-40 to +85	℃
T_J	Junction Temperature		-40 to +150	℃
T_{STG}	Storage Temperature Range		-65 to +150	℃

Note1. Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Note2. The value of V_{CCA} and V_{CCB} are provided in the recommended operating conditions table.

Recommended Operating Conditions (Note 1, 2)

Symbol	Parameter		V_{CCA}	V_{CCB}	Min	Max	Unit
V_{CCA}	Supply Voltage				1.2	3.6	V
V_{CCB}					1.65	5.5	V
V_{IH}	High Level Input Voltage	A- Port	1.65V to 1.95V	2.3V to 5.5V	V_{CCI} -0.2	V_{CCI}	
			2.3V to3.6V		V_{CCI} -0.4	V_{CCI}	
		B- Port	1.65V to 3.6V	2.3V to 5.5V	V_{CCI} -0.4	V_{CCI}	V
		OE			V_{CCA}×0.65	5.5	V
V_{IL}	Low Level Input Voltage	A- Port	1.65V to 3.6V	2.3V to 5.5V	0	0.15	
		B- Port			0	0.15	V
		OE			0	V_{CCA}×0.35	V
Δt/Δv	Input Transition Rise or Fall Time	A-Port push-pull driving	1.65V to 3.6V	2.3V to 5.5V		10	
		B-Port push-pull driving				10	ns/V
		Control input				10	

Note1. V_{CCI} is the supply voltage associated with the input port.

Note2. V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

Thermal Information

Thermal Metric	UM3284Q	UM3284QT	UM3284UE	Unit
$R_{\theta JA}$	52.8	119.8	41.9	°C/W
$R_{\theta JC}$	27.7	42.6	32.8	

Electrical Characteristics (Note 1, 2, 3)

Over recommended operating free-air temperature range (unless otherwise noted)

Parameter		Test Conditions	V_{CCA}	V_{CCB}	T_A=25℃		-40℃ to 85℃		Unit
					Typ	Max	Min	Max	
V_{OHA}		I_{OH}=-20μA V_{IB}≥V_{CCB}-0.4V	1.4V	1.65V to 5.5V	V_{CCA}×0.67				V
V_{OLA}		I_{OL}=180uA, V_{IB}≤0.15V	1.4V	1.65V to 5.5V				0.4	
		I_{OL}=220uA, V_{IB}≤0.15V	1.65V	1.65V to 5.5V				0.4	
		I_{OL}=300uA, V_{IB}≤0.15V	2.3V	1.65V to 5.5V				0.4	
		I_{OL}=400uA, V_{IB}≤0.15V	3V	1.65V to 5.5V				0.55	
V_{OHB}		I_{OH}=-20μA V_{IA}≥V_{CCA}-0.2V	1.4V	1.65V to 5.5V	V_{CCB}×0.67				V
V_{OLB}		I_{OL}=220uA, V_{IA}≤0.15V	1.4V to 3.6V	1.65				0.4	V
		I_{OL}=300uA, V_{IA}≤0.15V	1.4V to 3.6V	2.3				0.4	
		I_{OL}=400uA, V_{IA}≤0.15V	1.4V to 3.6V	3				0.55	
		I_{OL}=620uA, V_{IA}≤0.15V	1.4V to 3.6V	4.5				0.55	
I_I	OE	V_I=V_{CCI} or GND	1.4V	1.65V to 5.5V		±1		±2	μA
I_{OZ}	A or B Port	OE=V_{IL}	1.4V	1.65V to 5.5V		±1		±2	μA
I_{CCA}		V_I=V_O=open, I_O=0	1.4V to 3.6V	2.3V to 5.5V				2	μA
			3.6V	0V				2	
			0V	5.5V				-1	
I_{CCB}		V_I=V_O=open, I_O=0	1.4V to 3.6V	2.3V to 5.5V				6	
			3.6V	0V				-1	
			0V	5.5V				1.2	
I_{CCA} +I_{CCB}		V_I=V_O=open, I_O=0	1.4V	2.3V to 5.5V	3				
			1.5V to 3.6V	2.3V to 5.5V				8	μA
I_{CCZA}		V_I=V_O=open, I_O=0, OE=GND	1.4V	1.65V to 5.5V	0.05				
I_{CCZB}		V_I=V_O=open, I_O=0, OE=GND	1.4V	1.65V to 5.5V	4				
C_i	OE		3.3V	3.3V	4.5			6	pF
C_{iO}	A Port		3.3V	3.3V	6			8	pF
	B Port				5.5			7	

Note1. V_{CCI} is the supply voltage associated with the input port.
Note2. V_{CCO} is the supply voltage associated with the output port.
Note3. V_{CCA} must be less than or equal to V_{CCB} and must not exceed 3.6 V.

Timing Requirements

Over recommended operating free-air temperature range, VCCA= 1.5V±0.1V (unless otherwise noted)

			VCCB=1.8V ±0.15V		VCCB=2.5V ±0.2V		VCCB=3.3V ±0.3V		VCCB=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Rate	Push-pull			40		60		60		50	Mbps
	Open-drain			2		2		2		2	
t_w Pulse duration	Push-pull	Data inputs	25		16.7		16.7		20		ns
	Open-drain		500		500		500		500		

Timing Requirements

Over recommended operating free-air temperature range, VCCA= 1.8V±0.15V (unless otherwise noted)

			V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
Data Rate	Push-pull			40		60		60		60	Mbps
	Open-drain			2		2		2		2	
t_w Pulse duration	Push-pull	Data inputs	25		16.7		16.7		16.7		ns
	Open-drain		500		500		500		500		

Timing Requirements

Over recommended operating free-air temperature range, VCCA= 2.5V±0.2V (unless otherwise noted)

			V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	
Data Rate	Push-pull			60		60		60	Mbps
	Open-drain			2		2		2	
t_w Pulse duration	Push-pull	Data inputs	16.7		16.7		16.7		ns
	Open-drain		500		500		500		

Timing Requirements

Over recommended operating free-air temperature range, VCCA= 3.3V±0.3V (unless otherwise noted)

			V_{CCB}=3.3V±0.3V		V_{CCB}=5V±0.5V		Unit
			Min	Max	Min	Max	
Data Rate	Push-pull			60		60	Mbps
	Open-drain			2		2	
t_w Pulse duration	Push-pull	Data inputs	16.7		16.7		ns
	Open-drain		500		500		

Switching Characteristics

Over recommended operating free-air temperature range, V_{CCA}= 1.5V±0.1V (unless otherwise noted)

Parameter	Test Conditions		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}	A-B	Push-pull		12		10		9		9	ns
		Open-drain	4	21	3.6	20	3.5	19.5	3.5	19.5	
t_{PLH}	A-B	Push-pull		12		10		9.8		9.7	
		Open-drain	182	720	143	554	114	473	81	384	
t_{PHL}	B-A	Push-pull		12.7		11.1		11		12	ns
		Open-drain	3.4	20	3.1	14.5	2.8	11	2.5	7.5	
t_{PLH}	B-A	Push-pull		11		7		6.5		5.5	
		Open-drain	186	745	147	603	118	519	84	407	
t_{en}	OE-A OE-B	Push-pull		200		200		200		200	ns
t_{dis}	OE-A OE-B	Push-pull		150		150		150		150	ns
t_{rA}	A port rise time	Push-pull	3.5	13.1	3	9.8	3.1	9	3.2	8.3	ns
		Open-drain	147	982	115	716	92	592	66	481	
t_{rB}	B port rise time	Push-pull	2.9	11.4	1.9	9.1	0.9	4.7	0.7	2.6	ns
		Open-drain	135	1020	91	756	58	653	20	370	
t_{fA}	A port fall time	Push-pull	2.3	9.9	1.7	7.7	1.6	6.8	1.7	6	ns
		Open-drain	2.4	10	2.1	7.9	1.7	7	1.5	6.2	
t_{fB}	B port fall time	Push-pull	2	8.7	1.3	7	0.9	4.5	0.8	3.1	ns
		Open-drain	1.2	11.5	1.3	8.6	1	9.6	0.5	7.7	
$t_{SK(O)}$	Channel-to-Channel	Push-pull		1		1		1.1		1	ns
Max data rate	A or B	Push-pull	40		60		60		50		Mbps
		Open-drain	2		2		2		2		

Switching Characteristics

Over recommended operating free-air temperature range, V_{CCA}= 1.8V±0.15V (unless otherwise noted)

Parameter	Test Conditions		V_{CCB}=1.8V ±0.15V		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{PHL}	A-B	Push-pull		8.2		7.5		6.5		6.2	ns
		Open-drain	3.6	18	3.2	17	3.1	16	3.1	16	
t_{PLH}	A-B	Push-pull		9		7		6.5		6.3	
		Open-drain	194	729	155	584	126	466	90	346	
t_{PHL}	B-A	Push-pull		9.8		8		7.4		7	ns
		Open-drain	3.4	17.5	2.8	12.5	2.5	7.6	2.1	6.5	
t_{PLH}	B-A	Push-pull		10.2		7		5.8		5	
		Open-drain	197	733	159	578	129	459	93	323	
t_{en}	OE-A OE-B	Push-pull		200		200		200		200	ns
t_{dis}	OE-A OE-B	Push-pull		150		150		150		150	ns
t_{rA}	A port rise time	Push-pull	3.1	11.9	2.6	8.6	2.7	7.8	2.8	7.2	ns
		Open-drain	155	996	124	691	100	508	72	350	
t_{rB}	B port rise time	Push-pull	2.8	10.5	1.7	7.2	1.2	5.2	0.7	2.7	ns
		Open-drain	132	1001	106	677	73	546	32	323	
t_{fA}	A port fall time	Push-pull	2.1	8.8	1.6	6.6	1.4	5.7	1.4	4.9	ns
		Open-drain	2.2	9	1.7	6.7	1.4	5.8	1.5	5.2	
t_{fB}	B port fall time	Push-pull	2	8.3	1.3	5.4	0.9	3.9	0.7	3	ns
		Open-drain	0.8	10.5	0.7	10.7	1	9.6	0.6	7.8	
$t_{SK(O)}$	Channel-to-Channel	Push-pull		1		1		1.1		1	ns
Max data rate	A or B	Push-pull	40		60		60		60		Mbps
		Open-drain	2		2		2		2		

Switching Characteristics

Over recommended operating free-air temperature range, V_{CCA}= 2.5V±0.2V (unless otherwise noted)

Parameter	Test Conditions		V_{CCB}=2.5V ±0.2V		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	Min	Max	
t_{PHL}	A-B	Push-pull		5		4.6		4.1	ns
		Open-drain	2.4	13.6	2.3	13.5	2.2	13	
t_{PLH}	A-B	Push-pull		5.2		4.3		3.9	
		Open-drain	149	592	125	550	93	400	
t_{PHL}	B-A	Push-pull		5.4		4.7		4.2	ns
		Open-drain	2.5	10	2.2	9	1.8	6.5	
t_{PLH}	B-A	Push-pull		5.9		4.4		3.5	
		Open-drain	150	595	126	481	94	345	
t_{en}	OE-A OE-B	Push-pull		200		200		200	ns
t_{dis}	OE-A OE-B	Push-pull		150		150		150	ns
t_{rA}	A port rise time	Push-pull	2	7.3	2.1	6.4	2.2	5.8	ns
		Open-drain	110	692	93	529	68	369	
t_{rB}	B port rise time	Push-pull	1.8	6.5	1.3	5.1	0.7	3.4	ns
		Open-drain	107	693	79	483	41	304	
t_{fA}	A port fall time	Push-pull	1.5	5.7	1.2	4.7	1.3	3.8	ns
		Open-drain	1.5	5.6	1.2	4.7	1.1	4	
t_{fB}	B port fall time	Push-pull	1.4	5.4	0.9	4.1	0.7	3	ns
		Open-drain	0.4	14.2	0.5	19.4	0.4	3	
$t_{SK(O)}$	Channel-to-Channel	Push-pull		1		1.2		1	ns
Max data rate	A or B	Push-pull	60		60		60		Mbps
		Open-drain	2		2		2		

Switching Characteristics

Over recommended operating free-air temperature range, V_{CCA}= 3.3V±0.3V (unless otherwise noted)

Parameter	Test Conditions		V_{CCB}=3.3V ±0.3V		V_{CCB}=5V ±0.5V		Unit
			Min	Max	Min	Max	
t_{PHL}	A-B	Push-pull		3.8		3.5	ns
		Open-drain	2	8.4	1.9	8.2	
t_{PLH}	A-B	Push-pull		3.9		3.5	
		Open-drain	111	500	87	360	
t_{PHL}	B-A	Push-pull		4.2		3.8	ns
		Open-drain	2.1	6	1.7	5	
t_{PLH}	B-A	Push-pull		3.8		3.3	
		Open-drain	112	449	86	370	
t_{en}	OE-A OE-B	Push-pull		200		200	ns
t_{dis}	OE-A OE-B	Push-pull		150		150	ns
t_{rA}	A port rise time	Push-pull	1.8	5.7	1.9	5	ns
		Open-drain	75	446	57	337	
t_{rB}	B port rise time	Push-pull	1.5	5	1	3.6	ns
		Open-drain	72	427	40	290	
t_{fA}	A port fall time	Push-pull	1.2	4.5	1.1	3.5	ns
		Open-drain	1.1	4.4	1	3.7	
t_{fB}	B port fall time	Push-pull	1.1	4.2	0.8	3.1	ns
		Open-drain	1	4.2	0.8	3.1	
$t_{SK(O)}$	Channel-to-Channel	Push-pull		1		1	ns
Max data rate	A or B	Push-pull	60		60		Mbps
		Open-drain	2		2		

Applications Information

The UM3284 device is a directionless voltage-level translator specifically designed for translating logic voltage levels. The A-port accepts I/O voltages ranging from 1.2 V to 3.6 V. The B-port accepts I/O voltages from 1.65 V to 5.5 V. The device uses pass gate architecture with edge rate accelerators (one shots) to improve the overall data rate. The pull-up resistors, commonly used in open-drain applications, have been conveniently integrated so that an external resistor is not needed. While this device is designed for open-drain applications, the device can also translate push-pull CMOS logic outputs.

Block Diagram

Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE = Low.

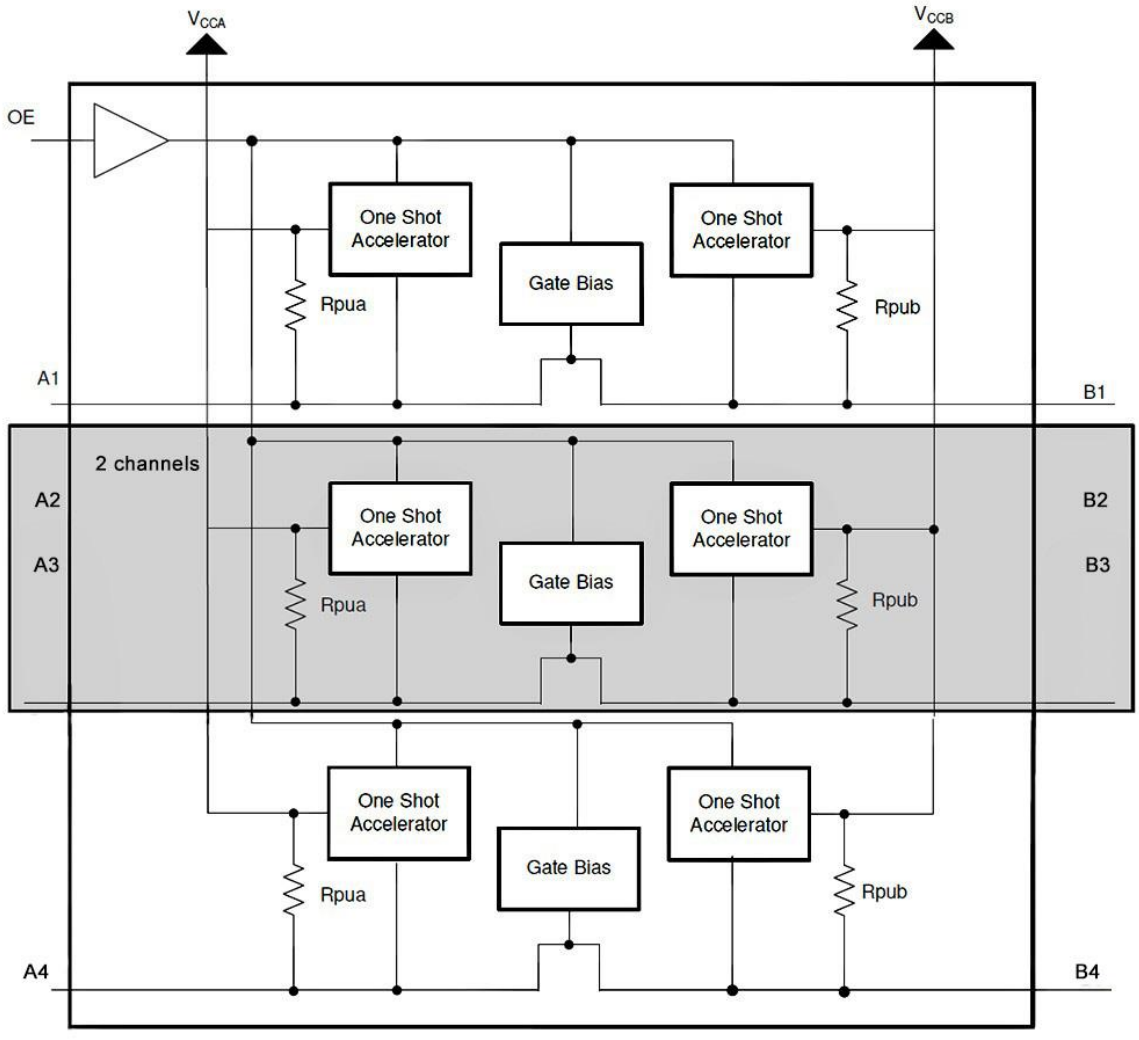


Figure 1 Block Diagram of UM3284 I/O Cell

Architecture

Figure 2 describes semi-buffered architecture design this application requires for both push-pull and open-drain mode. This application uses edge-rate accelerator circuitry (for both the high-to-low and low-to-high edges), a high-on-resistance N-channel pass-gate transistor (on the order of 300 Ω to 500 Ω) and pull-up resistors (to provide DC-bias and drive capabilities) to meet these requirements. This design needs no direction-control signal (to control the direction of data flow from A to B or from B to A). The resulting implementation supports both low- speed open-drain operation as well as high-speed push-pull operation.

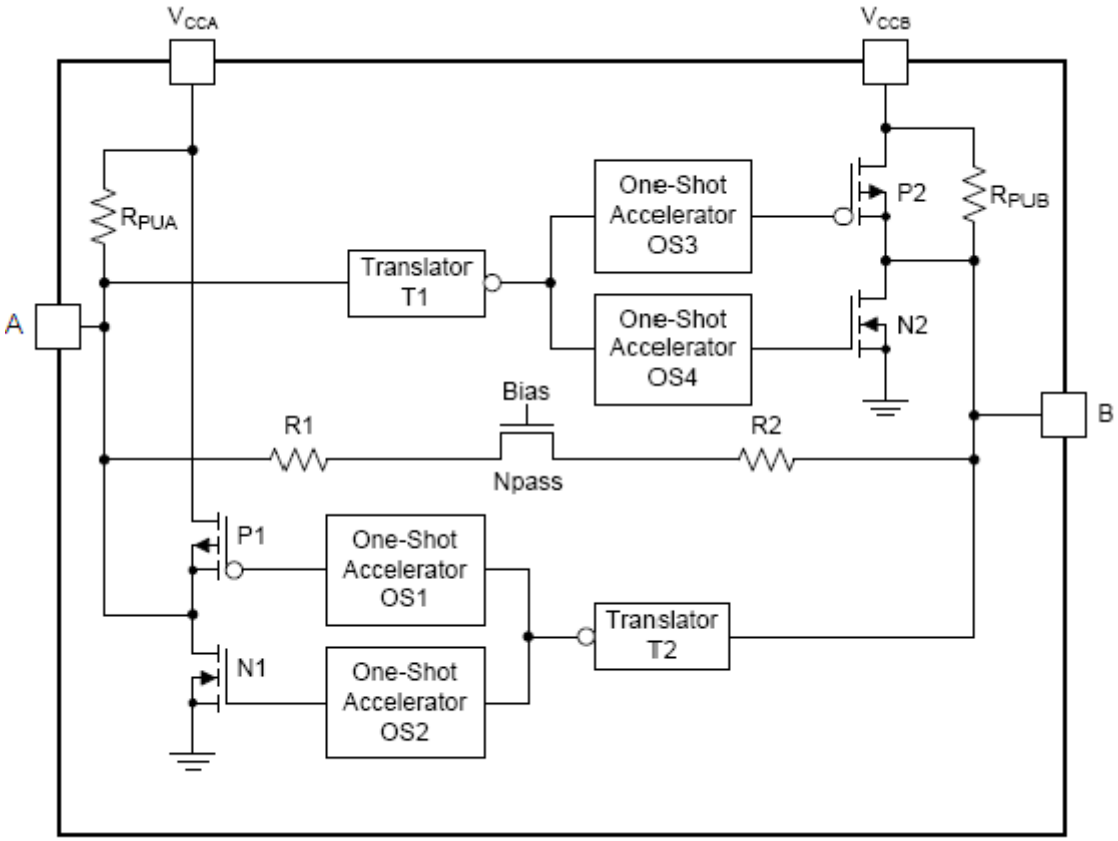


Figure 2 Architecture of UM3284 I/O Cell

When transmitting data from A-ports to B-ports, during a rising edge the one-shot circuit (OS3) turns on the PMOS transistor (P2) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from A to B, the one-shot circuit (OS4) turns on the N-channel MOSFET transistor (N2) for a short-duration which speeds up the high-to-low transition. The B-port edge-rate accelerator consists of one-shot circuits OS3 and OS4. Transistors P2 and N2 and serves to rapidly force the B port high or low when a corresponding transition is detected on the A port.

When transmitting data from B- to A-ports, during a rising edge the one-shot circuit (OS1) turns on the PMOS transistor (P1) for a short-duration which reduces the low-to-high transition time. Similarly, during a falling edge, when transmitting data from B to A, the one-shot circuit (OS2) turns on NMOS transistor (N1) for a short-duration and this speeds up the high-to-low transition. The A-port edge-rate accelerator consists of one-shots OS1 and OS2, transistors P1 and N1 components and form the edge-rate accelerator and serves to rapidly force the A port high or low when a corresponding transition is detected on the B port.

Input Driver Requirements

The continuous DC-current sinking capability is determined by the external system-level open-drain (or push-pull) drivers that are interfaced to the UM3284 I/O pins. Because the high bandwidth of these bidirectional I/O circuits is used to facilitate this fast change from an input to an output and an output to an input, they have a modest DC-current sourcing capability of hundreds of micro-amperes, as determined by the internal pull-up resistors.
The fall time (t_{fA}, t_{fB}) of a signal depends on the edge-rate and output impedance of the external device driving UM3284 data I/Os, as well as the capacitive loading on the data lines.
Similarly, the t_{PHL} and maximum data rates also depend on the output impedance of the external driver. The values for t_{fA}, t_{fB}, t_{PHL}, and maximum data rates in the data sheet assume that the output impedance of the external driver is less than 50Ω.

Output Load Considerations

Union recommends careful PCB layout practices with short PCB trace lengths to avoid excessive capacitive loading and to ensure that proper one-shot triggering takes place. PCB signal trace-lengths should be kept short enough such that the round trip delay of any reflection is less than the one-shot duration. This improves signal integrity by ensuring that any reflection sees a low impedance at the driver. The one-shot circuits have been designed to stay on for approximately 30 ns. The maximum capacitance of the lumped load that can be driven also depends directly on the one-shot duration. With very heavy capacitive loads, the one-shot can time-out before the signal is driven fully to the positive rail. The one-shot duration has been set to best optimize trade-offs between dynamic I_{CC}, load driving capability, and maximum bit-rate considerations. Both PCB trace length and connectors add to the capacitance of the UM3284 output. Therefore, Union recommends that this lumped-load capacitance is considered in order to avoid one-shot retriggering, bus contention, output signal oscillations, or other adverse system-level affects.

Enable and Disable

The UM3284 has an OE pin input that is used to disable the device by setting the OE pin low, which places all I/Os in the Hi-Z state. The disable time (tdis) indicates the delay between the time when the OE pin goes low and when the outputs actually get disabled (Hi-Z). The enable time (ten) indicates the amount of time the design must allow for the one-shot circuitry to become operational after the OE pin goes high.

Pull-up or Pull-down Resistors on I/O Lines

The UM3284 has the smart pull-up resistors dynamically change value based on whether a low or a high is being passed through the I/O line. Each A-port I/O has a pull-up resistor (R_{PUA}) to V_{CCA} and each B-port I/O has a pull-up resistor (R_{PUB}) to V_{CCB}. R_{PUA} and R_{PUB} have a value of 40kΩ when the output is driving low. R_{PUA} and R_{PUB} have a value of 4kΩ when the output is driving high. R_{PUA} and R_{PUB} are disabled when OE=Low. This feature provides lower static power consumption (when the I/Os are passing a low), and supports lower V_{OL} values for the same size pass-gate transistor, and helps improve simultaneous switching performance.

Device Functional Modes

The UM3284 device has two functional modes, enabled and disabled. To disable the device set the OE pin input low, which places all I/Os in a high impedance state. Setting the OE pin input high enables the device.

Typical Operating Circuit

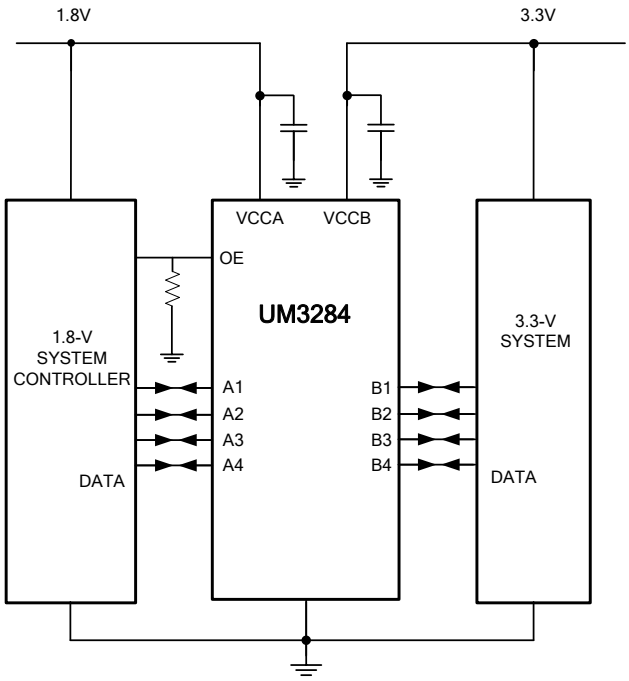
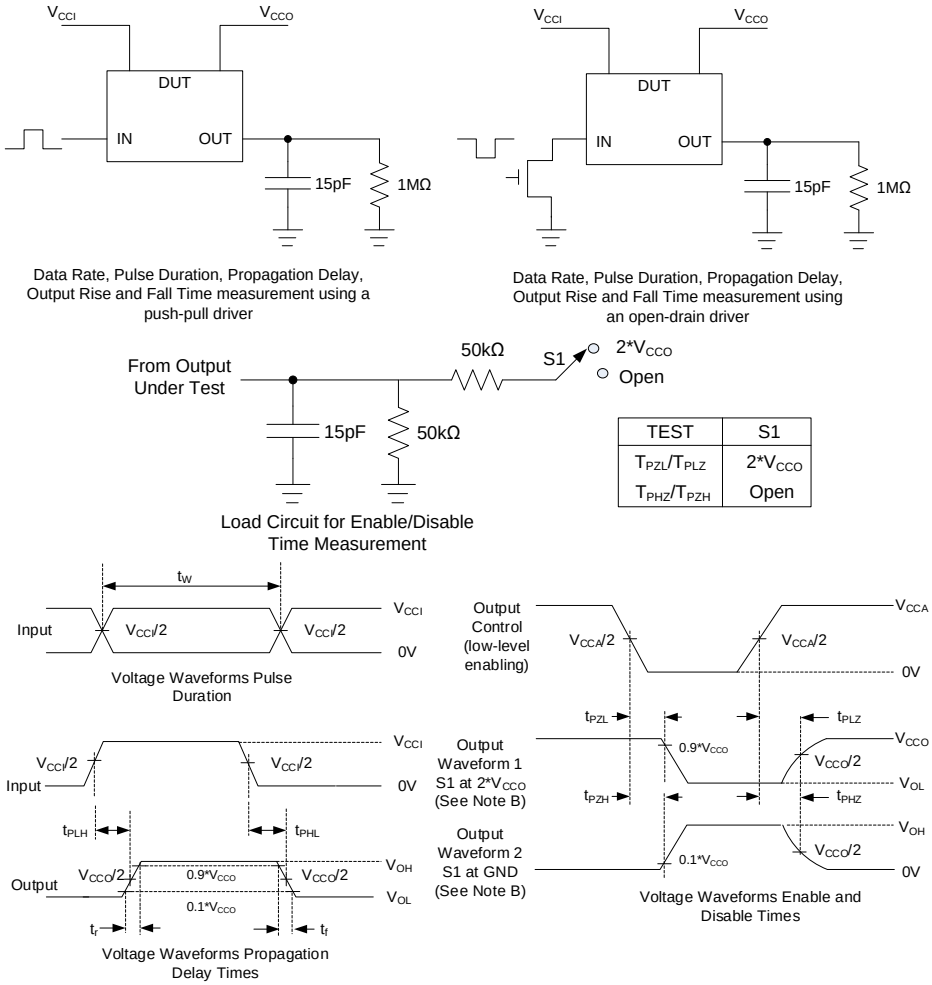


Figure 3 Typical Operating Circuit

Test Circuits



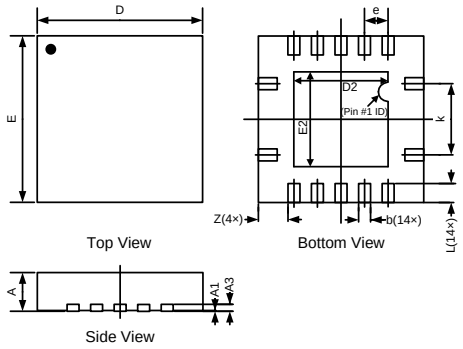
A. C_L includes probe and jig capacitances.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤100MHz, Z_O=50Ω, dv/dt≥1V/ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. T_{PLZ} and T_{PHZ} are the same as tdis.
F. T_{PZL} and T_{PZH} are the same as ten.
G. T_{PLH} and T_{PHL} are the same as tpd.
H. V_{CCI} is the V_{CC} associated with the input port.
I. V_{CCO} is the V_{CC} associated with the output port.
J. All parameters and waveforms are not applicable to all devices.

Figure 4 Load Circuits and Voltage Waveforms

Package Information

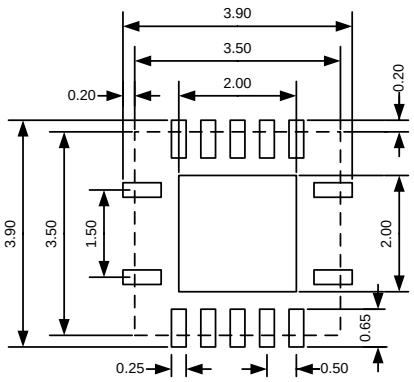
UM3284Q QFN14 3.5×3.5

Outline Drawing



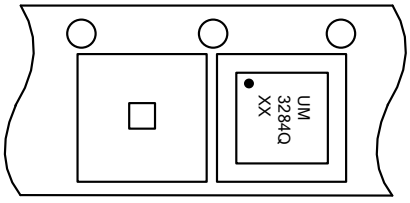
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	0.75	0.80	0.85	0.030	0.031	0.033
A1	0.00	0.02	0.05	0.000	0.0008	0.002
A3	0.15REF			0.006REF		
b	0.20	0.25	0.30	0.008	0.010	0.012
D	3.45	3.50	3.55	0.136	0.138	0.140
D2	1.90	2.00	2.10	0.075	0.079	0.083
E	3.45	3.50	3.55	0.136	0.138	0.140
E2	1.90	2.00	2.10	0.075	0.079	0.083
e	0.50BSC			0.020BSC		
k	1.50TYP			0.059TYP		
L	0.35	0.40	0.45	0.014	0.016	0.018
Z	0.625TYP			0.025TYP		

Land Pattern



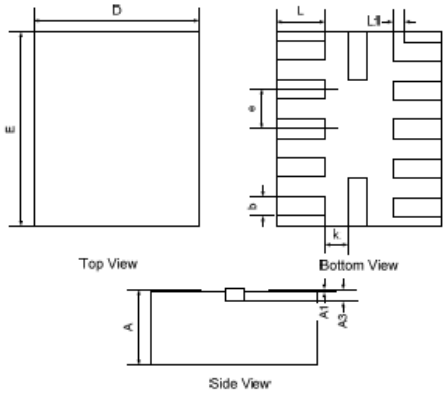
NOTES:
1. Compound dimension: 3.50×3.50;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



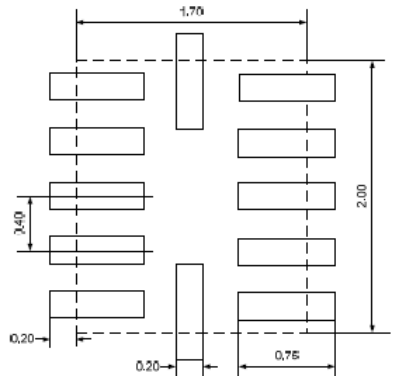
UM3284QT QFN12 1.7×2.0

Outline Drawing



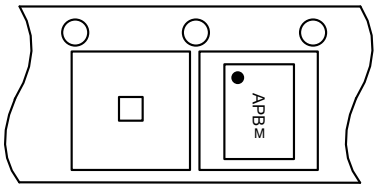
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	>0.5	0.55	0.60	>0.020	0.022	0.024
A1	0.00	-	0.05	0.000	-	0.002
A3	0.15REF			0.006REF		
b	0.15	0.20	0.25	0.006	0.008	0.010
D	1.75	1.80	1.85	0.069	0.071	0.073
E	2.55	2.60	2.65	0.100	0.102	0.104
e	0.40BSC			0.016BSC		
L	0.30	0.40	0.50	0.012	0.016	0.020

Land Pattern



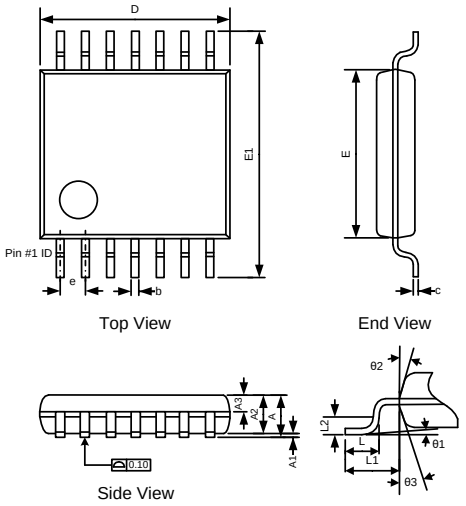
NOTES:
1. Compound dimension: 1.7×2.0 ;
2. Unit: mm;
3.General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



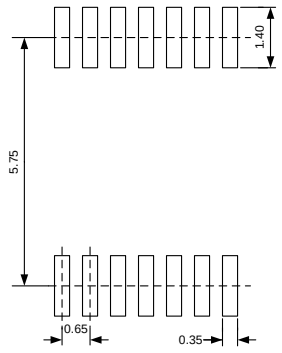
UM3284UE TSSOP14

Outline Drawing



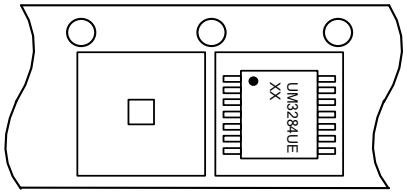
DIMENSIONS						
Symbol	MILLIMETERS			INCHES		
	Min	Typ	Max	Min	Typ	Max
A	-	-	1.20	-	-	0.047
A1	0.05	-	0.15	0.002	-	0.006
A2	0.90	1.00	1.05	0.035	0.039	0.041
A3	0.34	0.44	0.54	0.013	0.017	0.021
b	0.20	-	0.28	0.008	-	0.011
c	0.10	-	0.19	0.004	-	0.007
D	4.86	4.96	5.06	0.191	0.195	0.199
E	4.30	4.40	4.50	0.169	0.173	0.177
E1	6.20	6.40	6.60	0.244	0.252	0.260
e	0.65BSC			0.026BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		
L2	0.25BSC			0.010BSC		
θ1	0°	-	8°	0°	-	8°
θ2	10°	12°	14°	10°	12°	14°
θ3	10°	12°	14°	10°	12°	14°

Land Pattern



NOTES:
1. Compound dimension: 4.96×4.40;
2. Unit: mm;
3. General tolerance ±0.05mm unless otherwise specified;
4. The layout is just for reference.

Tape and Reel Orientation



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